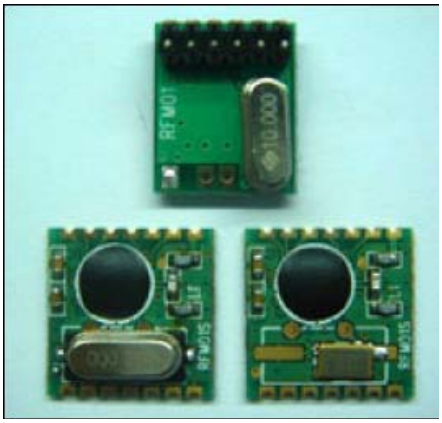
Old Version

RFM01 Universal ISM Band FSK Receiver

RFM01



DESCRIPTION

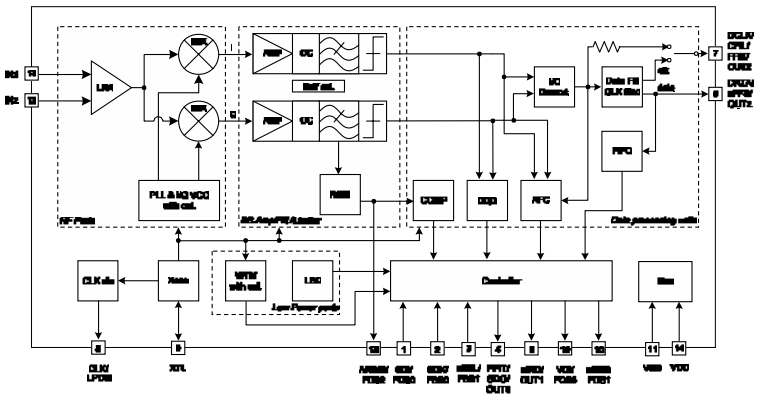
Hoperf' RFM01 is a single module, low power, multi-channel FSK receiver designed for use in applications requiring FCC or ETSI conformance for unlicensed use in the 315, 433, 868, and 915 MHz bands. Used in conjunction with RFM02, Hoperf' FSK transmitters, the RFM01 is a flexible, low cost, and highly integrated solution that does not require production alignments. All required RF functions are integrated. Only an external crystal and bypass filtering are needed for operation.

The RFM01 has a completely integrated PLL for easy RF design, and its rapid settling time allows for fast frequency hopping, bypassing multipath fading, and interference to achieve robust wireless links. The PLL's high resolution allows the usage of multiple channels in any of the bands. The baseband bandwidth (BW) is programmable to accommodate various deviation, data rate, and crystal tolerance requirements. The receiver employs the Zero-IF approach with I/Q demodulation, therefore no external components (except crystal and decoupling) are needed in a typical application. The RFM01 is a complete analog RF and baseband receiver including a multi-band PLL synthesizer with an LNA, I/Q down converter mixers, baseband filters and amplifiers, and I/Q demodulator.

The Module dramatically reduces the load on the microcontroller with integrated digital data processing: data filtering, clock recovery, data pattern recognition and integrated FIFO. The automatic frequency control (AFC) feature allows using a low accuracy (low cost) crystal. To minimize the system cost, the chip can provide a clock signal for the microcontroller, avoiding the need for two crystals.

For simple applications, the receiver supports a standalone operation mode. This allows complete data receiver operation and control of four digital outputs based on the incoming data pattern without a microcontroller. In this mode, 12 or more predefined frequency channels can be used in any of the four bands. For low power applications, the device supports low duty-cycle operation based on the internal wake-up timer.

FUNCTIONAL BLOCK DIAGRAM



FEATURES

- Fully integrated (low BOM, easy design-in)
- No alignment required in production
- Fast settling, programmable, high-resolution PLL
- Fast frequency hopping capability
- High bit rate (up to 115.2 kbps in digital mode and 256 kbps in analog mode)
- Direct differential antenna input
- Programmable baseband bandwidth (67 to 400 kHz)
- Analog and digital RSSI outputs
- Automatic frequency control (AFC)
- Data quality detection (DQD)
- Internal data filtering and clock recovery
- RX pattern recognition
- SPI compatible serial control interface
- Clock and reset signals for microcontroller
- 16 bit RX data FIFO
- Standalone operation mode without microcontroller
- Low power duty-cycle mode (less than 0.5 mA average supply current)
- Standard 10 MHz crystal reference with in circuit calibration
- Alternative OOK support
- Wake-up timer
- Low battery detector
- 2.2 to 5.4 V supply voltage
- Low power consumption (~9 mA in low bands)
- Low standby current (0.3 μA)
- Compact 16-pin TSSOP package

TYPICAL APPLICATIONS

- Remote control
- Home security and alarm
- Wireless keyboard/mouse and other PC peripherals
- Toy control
- Remote keyless entry
- Tire pressure monitoring
- Telemetry
- Personal/patient data logging
- Remote automatic meter reading

DETAILED DESCRIPTION

General

The RFM01 FSK receiver is the counterpart of the RFM01 FSK transmitter. It covers the unlicensed frequency bands at 315, 433, 868, and 915 MHz. The device facilitates compliance with FCC and ETSI requirements.

The receiver employs the Zero-IF approach with I/Q demodulation, allowing the use of a minimal number of external components in a typical application. The RFM01 consists of a fully integrated multi-band PLL synthesizer, an LNA with switchable gain, I/Q down converter mixers, baseband filters and amplifiers, and an I/Q demodulator followed by a data filter.

PLL

The programmable PLL synthesizer determines the operating frequency, while preserving accuracy based on the on-chip crystal-controlled reference oscillator. The PLL's high resolution allows for the use of multiple channels in any of the bands.

The RF VCO in the PLL performs automatic calibration, which requires only a few microseconds. Calibration always occurs when the synthesizer begins. If temperature or supply voltage changes significantly or operational band has changed, VCO recalibration is recommended. Recalibration can be initiated at any time by switching the synthesizer off and back on again.

LNA

The LNA has 250 Ohm input impedance, which works well with the recommended antennas.

If the RF input of the chip is connected to 50 Ohm devices, an external matching circuit is required to provide the correct matching and to minimize the noise figure of the receiver.

The LNA gain (and linearity) can be selected (0, –6, –14, –20 dB relative to the highest gain) according to RF signal strength. This is useful in an environment with strong interferers.

Baseband Filters

The receiver bandwidth is selectable by programming the bandwidth (BW) of the baseband filters. This allows setting up the receiver according to the characteristics of the signal to be received.

An appropriate bandwidth can be selected to accommodate various FSK deviation, data rate, and crystal tolerance requirements. The filter structure is a 7-th order Butterworth low-pass with 40 dB suppression at 2*BW frequency. Offset cancellation is accomplished by using a high-pass filter with a cut-off frequency below 7 kHz. See Measurement Results section for measured receiver selectivity curves.

Data Filtering and Clock Recovery

The output data filtering can be completed by an external capacitor or by using digital filtering according to the final application.

Analog operation: The filter is an RC type low-pass filter and a Schmitt-trigger (St). The resistor (10k) and the St is integrated on the chip. An (external) capacitor can be chosen according to the actual bit-rate. In this mode the receiver can handle up to 256 kbps data rate.

Digital operation: The data filter is a digital realization of an analog RC filter followed by a comparator with hysteresis. In this mode there is a clock recovery circuit (CR), which can provide synchronized clock to the data. With this clock the received data can fill the RX Data FIFO. The CR has three operation modes: fast, slow, and automatic. In slow mode, its noise immunity is very high, but it has slower settling time and requires more accurate data timing than in fast mode. In automatic mode the CR automatically changes between fast and slow modes. The CR starts in fast mode, then automatically switches to slow mode after locking.

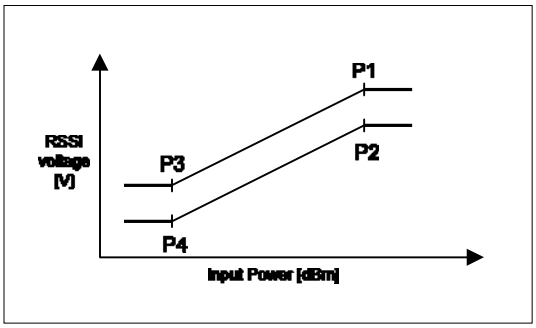
(Only the data filter and the clock recovery use the bit-rate clock. Therefore, in analog mode, there is no need for setting the correct bit-rate.)

Data Validity Blocks

RSSI

A digital RSSI output is provided to monitor the input signal level. It goes high if the received signal strength exceeds a given preprogrammed level. An analog RSSI signal is also available. The RSSI settling time depends on the filter capacitor used.

Voltage on ARRSI pin vs. Input RF power



P1	-65 dBm	1300 mV
P2	-65 dBm	1000 mV
P3	-100 dBm	600 mV
P4	-100 dBm	300 mV

DQD

The Data Quality Detector monitors the I/Q output of the baseband amplifier chain by counting the consecutive correct 0->1, 1->0 transitions. The DQD output indicates the quality of the signal to be demodulated. Using this method it is possible to "forecast" the probability of BER degradation. The programmable DQD parameter defines the threshold for signaling the good/bad data quality by the digital one-bit DQD output. In cases when the deviation is close to the bitrate, there should be four transitions during a single one bit period in the I/Q signals. As the bitrate decreases in comparison to the deviation, more and more transitions will happen during a bitperiod.

AFC

By using an integrated Automatic Frequency Control (AFC) feature, the receiver can synchronize its local oscillator to the received signal, allowing the use of:

- inexpensive, low accuracy crystals
- narrower receiver bandwidth (i.e. increased sensitivity)
- higher data rate

Crystal Oscillator

The chip has a single-pin crystal oscillator circuit, which provides a 10 MHz reference signal for the PLL. To reduce external parts and simplify design, the crystal load capacitor is internal and programmable. Guidelines for selecting the appropriate crystal can be found later in this datasheet. The receiver can supply the clock signal for the microcontroller, so accurate timing is possible without the need for a second crystal.

When the microcontroller turns the crystal oscillator off by clearing the appropriate bit using the Configuration Setting Command, the chip provides a fixed number (128) of further clock pulses (“clock tail”) for the microcontroller to let it go to idle or sleep mode.

Low Battery Voltage Detector

The low battery detector circuit monitors the supply voltage and generates an interrupt if it falls below a programmable threshold level. The detector circuit has 50 mV hysteresis.

Wake-Up Timer

The wake-up timer has very low current consumption (1.5 µA typical) and can be programmed from 1 ms to several days with an accuracy of ±10%.

It calibrates itself to the crystal oscillator at every startup. When the crystal oscillator is switched off, the calibration circuit switches it back on only long enough for a quick calibration (a few milliseconds) to facilitate accurate wake-up timing.

Event Handling

In order to minimize current consumption, the receiver supports the sleep mode. Active mode can be initiated by several wake-up events (wake-up timer timeout, low supply voltage detection, on-chip FIFO filled up or receiving a request through the serial interface).

If any wake-up event occurs, the wake-up logic generates an interrupt signal, which can be used to wake up the microcontroller, effectively reducing the period the microcontroller has to be active. The cause of the interrupt can be read out from the receiver by the microcontroller through the SDO pin.

Interface and Controller

An SPI compatible serial interface lets the user select the frequency band, center frequency of the synthesizer, and the bandwidth of the baseband signal path. Division ratio for the microcontroller clock, wake-up timer period, and low supply voltage detector threshold are also programmable. Any of these auxiliary functions can be disabled when not needed. All parameters are set to default after power-on; the programmed values are retained during sleep mode. The interface supports the read-out of a status register, providing detailed information about the status of the receiver and the received data. It is also possible to store the received data bits into the 16bit RX FIFO register and read them out in a buffered mode. FIFO mode can be enabled through the SPI compatible interface by setting the *fe* bit to 1 in the Output and FIFO Mode Command.

Standalone Operation Mode

The chip also provides a standalone mode, which allows the use of the receiver without a microcontroller. This mode can be selected by connecting the CLK/LPDM pin to either VDD or VSS. After power on, the chip will check this pin. If it is connected to any supply voltage, then the chip will go to standalone mode. Otherwise, it will go to microcontroller mode and the pin will become an output and provide a clock signal for the microcontroller. To prevent the RFM01 from accidentally entering a standalone mode, the stray capacitance should be kept below 50 pF on pin 8.

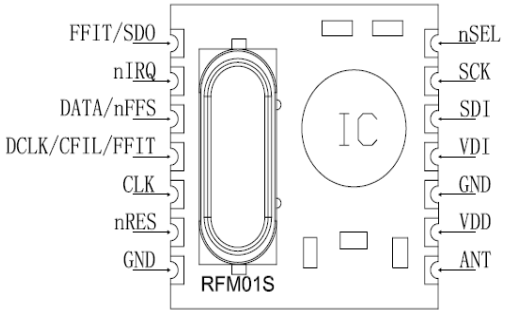
In this mode operating parameters can be selected from a limited set by “programming” the receiver over its pins. The chip is addressable and four digital output pins can be controlled by the received data. Selecting the Low Power Duty-Cycle Mode (LPDM) the chip consumes less than 0.5 mA average current.

PACKAGE PIN DEFINITIONS, MICROCONTROLLER MODE

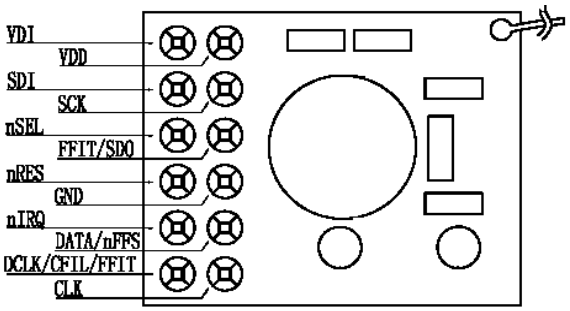
Pin type key: D=digital, A=analog, S=supply, I=input, O=output, IO=input/output

Microcontroller Mode Pin Assignment

SMD



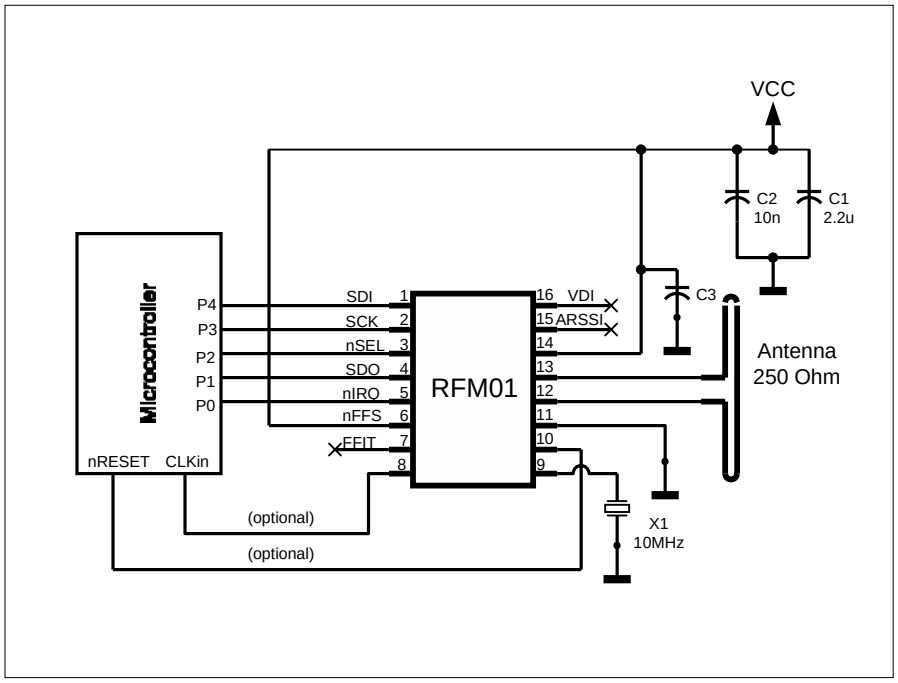
DIP



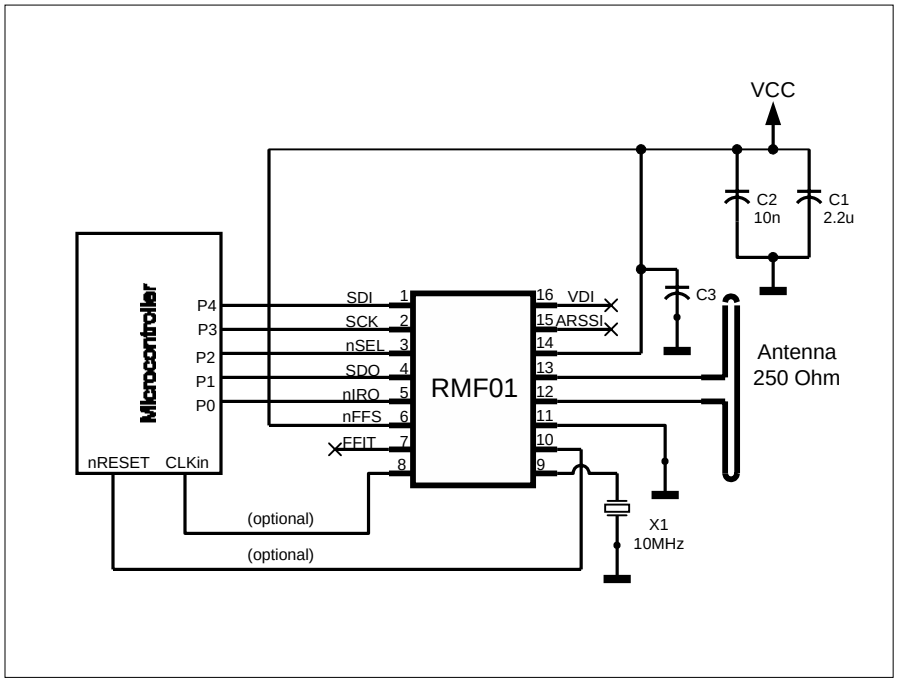
Pin	Name	Type	Function
1	SDI	DI	Data input of serial control interface
2	SCK	DI	Clock input of serial control interface
3	nSEL	DI	Chip select input of three-wire control interface (active low)
4	FFIT/SDO	DO	FIFO IT (active low) or serial data out for Status Read Command. Tristate with bushold cell if nSEL=H
5	nIRQ	DO	Interrupt request output, (active low)
6	DATA	DO	Received data output (FIFO not used)
	nFFS	DI	FIFO select input (active low)
7	DCLK	DO	Received data clock output (Digital filter used, FIFO not used)
	CFIL	AIO	External data filter capacitor connection (Analog filter used)
	FFIT	DO	FIFO IT (active high) FIFO empty function can be achieved when FIFO IT level is set to one
8	CLK	DO	Clock output for the microcontroller
9	XTL/REF	AIO	Crystal connection (other terminal of crystal to VSS) / External reference input
10	nRES	DO	Reset output (active low)
11	VSS	S	Negative supply voltage
12	IN2	AI	RF differential signal input
13	IN1	AI	RF differential signal input
14	VDD	S	Positive supply voltage
15	ARSSI	AO	Analog RSSI output
16	VDI	DO	Valid Data Indicator output

Typical Application, Microcontroller Mode

Minimal Microcontroller Mode



Microcontroller Mode with FIFO usage



Recommended supply decoupling capacitor values

C2 and C3 should be 0603 size ceramic capacitors to achieve the best supply decoupling. The capacitor values are valid for both stand-alone and microcontroller mode.

Band [MHz]	C1	C2	C3
315	2.2µF	10nF	390pF
433	2.2µF	10nF	220pF
868	2.2µF	10nF	47pF
915	2.2µF	10nF	33pF

GENERAL DEVICE SPECIFICATIONS

All voltages are referenced to V_{ss}, the potential on the ground reference pin VSS.

Absolute Maximum Ratings (non-operating)

Symbol	Parameter	Min	Max	Units
V_{dd}	Positive supply voltage	-0.5	6.0	V
V_{in}	Voltage on any pin except open collector outputs	-0.5	V_{dd}+0.5	V
I_{in}	Input current into any pin except VDD and VSS	-25	25	mA
ESD	Electrostatic discharge with human body model		1000	V
T_{st}	Storage temperature	-55	125	ºC
T_{ld}	Lead temperature (soldering, max 10 s)		260	ºC

Recommended Operating Range

Symbol	Parameter	Min	Max	Units
V_{dd}	Positive supply voltage	2.2	5.4	V
T_{op}	Ambient operating temperature	-40	85	ºC

ELECTRICAL SPECIFICATION

(Test Conditions: T_{op} = 27 ºC; V_{dd} = V_{oc} = 3.3 V)

DC Characteristics

Symbol	Parameter	Conditions/Notes	Min	Typ	Max	Units
I_{dd}	Supply current	315 / 433 MHz bands		9	11	mA
		868 MHz band		10.5	12.5	
		915 MHz band		12	14	
I_{pd}	Standby current	All blocks disabled		0.3		µA
I_{lb}	Low battery voltage detector current consumption			0.5		µA
I_{wt}	Wake-up timer current consumption (Note 1)			1.5		µA
I_x	Idle current	Crystal oscillator and base band parts are ON		3.0	3.5	mA
V_{lb}	Low battery detect threshold	Programmable in 0.1 V steps	2.25		5.35	V
V_{lba}	Low battery detection accuracy			+/-3		%
V_{il}	Digital input low level				0.3*V_{dd}	V
V_{ih}	Digital input high level		0.7*V_{dd}			V
I_{il}	Digital input current	V_{il} = 0 V	-1		1	µA
I_{ih}	Digital input current	V_{ih} = V_{dd}, V_{dd} = 5.4 V	-1		1	µA
V_{ol}	Digital output low level	I_{ol} = 2 mA			0.4	V
V_{oh}	Digital output high level	I_{oh} = -2 mA	V_{dd}-0.4			V

Note 1: **Using the internal wake-up timer and counter reduces the overall current consumption, which should permit approximately 6 months operation from a 1500mAh battery.**

AC Characteristics

Symbol	Parameter	Conditions/Notes	Min	Typ	Max	Units
f_{LO}	Receiver frequency	315 MHz band, 2.5 kHz resolution	310.24		319.75	MHz
		433 MHz band, 2.5 kHz resolution	430.24		439.75	
		868 MHz band, 5.0 kHz resolution	860.48		879.51	
		915 MHz band, 7.5 kHz resolution	900.72		929.27	
BW	Base-band bandwidth	mode 0	60	67	75	kHz
		mode 1	120	134	150	
		mode 2	180	200	225	
		mode 3	240	270	300	
		mode 4	300	350	375	
		mode 5	360	400	450	
BR	FSK bit rate	With internal digital filters			115.2	kbps
BRA	FSK bit rate	With analog filter			256	kbps
P_{min}	Receiver Sensitivity	BER 10^{-3}, BW=67 kHz, BR=1.2 kbps (Note 1)		-109	-100	dBm
AFC_{range}	AFC locking range	δf_{FSK}: FSK deviation in the received signal		$0.8*\delta f_{FSK}$		
$IIP3_{inh}$	Input IP3	In band interferers in high bands		-21		dBm
$IIP3_{outh}$	Input IP3	Out of band interferers $f\text{-}f_{LO} > 4MHz$		-18		dBm
$IIP3_{inl}$	IIP3 (LNA –6dB gain)	In band interferers in low bands		-15		dBm
$IIP3_{outl}$	IIP3 (LNA –6dB gain)	Out of band interferers $f\text{-}f_{LO} > 4MHz$		-12		dBm
P_{max}	Maximum input power	LNA: high gain	0			dBm
Rin	RF input impedance real part (differential) (Note 2)	LNA gain (0, -14dB) LNA gain (-6, -20dB)		250 500		Ohm
Cin	RF input capacitance			1		pF
RS_a	RSSI accuracy			+/-5		dB
RS_r	RSSI range			46		dB
C_{ARSSI}	Filter cap for ARSSI		1			nF
RS_{step}	RSSI programmable level steps			6		dB
RS_{resp}	DRSSI response time	Until the RSS output goes high after the input signal exceeds the preprogrammed limit C_{ARRSI}=5nF		500		µs

Note 1: **See the BER diagrams in the measurement results section for detailed information.**

Note 2: **See matching circuit parameters and antenna design guide for information, and Application Notes available from www.hoperf.com.**

AC Characteristics (continued)

Symbol	Parameter	Conditions/Notes	Min	Typ	Max	Units
f_{ref}	PLL reference frequency	(Note 3)	8	10	12	MHz
f_{res}	PLL frequency resolution	Depends on selected bands	2.5		7.5	kHz
t_{lock}	PLL lock time	Frequency error < 1kHz after 10 MHz step		20		µs
$t_{st, P}$	PLL startup time	With running crystal oscillator			250	µs
C_{xl}	Crystal load capacitance, see crystal selection guide	Programmable in 0.5 pF steps, tolerance +/- 10%	8.5		16	pF
t_{POR}	Internal POR pulse width (Note 4)	After V_{dd} has reached 90% of final value		50	150	ms
t_{sx}	Crystal oscillator startup time	Crystal ESR < 100 Ohms (Note 5)		1	5	ms
t_{PBt}	Wake-up timer accuracy	Crystal oscillator must be enabled to ensure proper calibration at startup (Note 5)		+/-10		%
$t_{wake-up}$	Programmable wake-up time		1		$5 \cdot 10^{11}$	ms
$C_{in, D}$	Digital input capacitance				2	pF
$t_{r, f}$	Digital output rise/fall time	15 pF pure capacitive load			10	ns

Note 3: Using other than a 10 MHz crystal is not recommended because the crystal referred timing and frequency parameters will change accordingly.

Note 4: During this period, commands are not accepted by the chip. For detailed information see the *Reset modes* section.

Note 5: The crystal oscillator start-up time strongly depends on the capacitance seen by the oscillator. Using low capacitance and low ESR crystal is recommended. When designing the PCB layout keep the trace connecting to the crystal short to minimize stray capacitance.

CONTROL INTERFACE

Commands to the receiver are sent serially. Data bits on pin SDI are shifted into the device upon the rising edge of the clock on pin SCK whenever the chip select pin nSEL is low. When the nSEL signal is high, it initializes the serial interface. The number of bits sent is an integer multiple of 8. All commands consist of a command code, followed by a varying number of parameter or data bits. All data are sent MSB first (e.g. bit 15 for a 16-bit command). Bits having no influence (don't care) are indicated with X. The Power On Reset (POR) circuit sets default values in all control registers.

The status information or received data can be read serially over the SDO pin. Bits are shifted out upon the falling edge of CLK signal. When the nSEL is high, the SDO output is in a high impedance state.

The receiver will generate an interrupt request (IRQ) for the microcontroller on the following events:

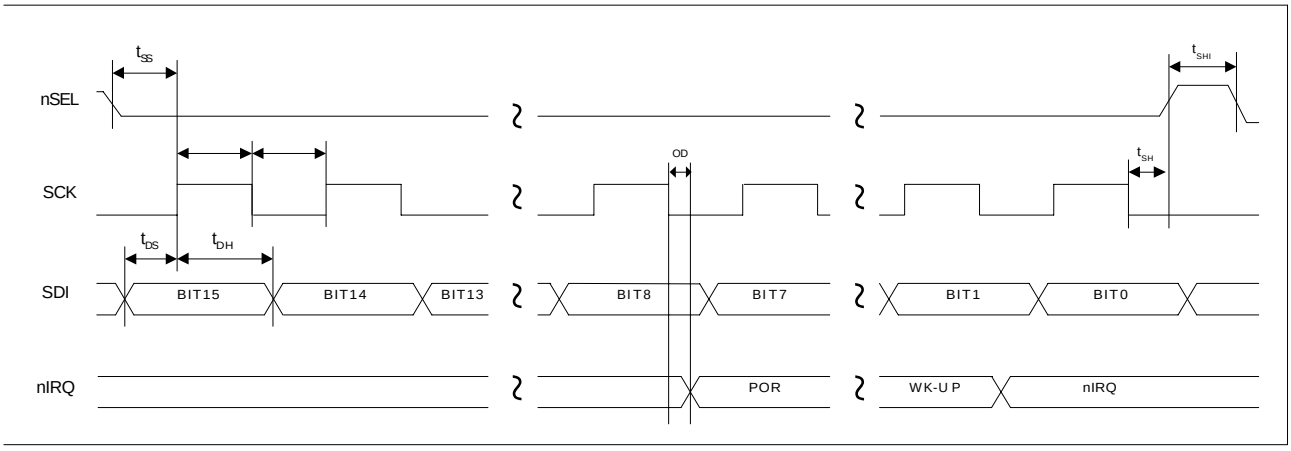
- Supply voltage below the preprogrammed value is detected (LBD)
- Wake-up timer timeout (WK-UP)
- FIFO received the preprogrammed amount of bits (FFIT)
- FIFO overflow (FFOV)

FFIT and FFOV are applicable only when the FIFO is enabled. To find out why the nIRQ was issued, the status bits should be read out.

Timing Specification

Symbol	Parameter	Minimum value [ns]
t_{CH}	Clock high time	25
t_{CL}	Clock low time	25
t_{SS}	Select setup time (nSEL falling edge to SCK rising edge)	10
t_{SH}	Select hold time (SCK falling edge to nSEL rising edge)	10
t_{SHI}	Select high time	25
t_{DS}	Data setup time (SDI transition to SCK rising edge)	5
t_{DH}	Data hold time (SCK rising edge to SDI transition)	5
t_{OD}	Data delay time	10

Timing Diagram



Control Commands

	Control Word	Related Parameters/Functions	Related Control Bits
1	Configuration Setting Command	Frequency band, low battery detector, wake-up timer, crystal oscillator load capacitance, baseband filter bandwidth, clock output	b1 to b0, eb, et, ex, x3 to x0, i2 to i0, dc
2	Frequency Setting Command	Set the frequency of the local oscillator	f11 to f0
3	Receiver Setting Command	Set VDI source, LNA gain, RSSI threshold,	d1 to d0, g1 to g0, r2 to r0, en
4	Wake-up Timer Command	Wake-up time period	r4 to r0, m7 to m0
5	Low Duty-Cycle Command	Set duty-cycle, enable low duty-cycle mode.	d6 to d0, en
6	Low Battery Detector and Clock Divider Command	Set LBD threshold voltage and microcontroller clock division ratio	d2 to d0, t4 to t0
7	AFC Control Command	Set AFC parameters	a1 to a0, rl1 to rl0, st, fi, oe, en
8	Data Filter Command	Set data filter type, clock recovery parameters	al, ml, s1 to s0, f2 to f0
9	Data Rate Command	Bit rate	cs, r6 to r0
10	Output and FIFO Command	Set FIFO IT level, FIFO start control, FIFO enable and FIFO fill enable	f3 to f0, s1 to s0, ff, fe
11	Reset Mode Command	Enable / disable sensitive reset	dr
12	Status Read Command	Read status information	

Note: In the following tables the POR column shows the default values of the command registers after power-on.

1. Configuration Setting Command

bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0	POR
	1	0	0	b1	b0	eb	et	ex	x3	x2	x1	x0	i2	i1	i0	dc	893Ah

b1	b0	Frequency Band [MHz]
0	0	315
0	1	433
1	0	868
1	1	915

i2	i1	i0	Baseband Bandwidth [kHz]
0	0	0	reserved
0	0	1	400
0	1	0	340
0	1	1	270
1	0	0	200
1	0	1	134
1	1	0	67
1	1	1	reserved

x3	x2	x1	x0	Crystal Load Capacitance [pF]
0	0	0	0	8.5
0	0	0	1	9.0
0	0	1	0	9.5
0	0	1	1	10.0
…				
1	1	1	0	15.5
1	1	1	1	16.0

Bits *eb* and *et* control the operation of the low battery detector and wake-up timer, respectively. They are enabled when the corresponding bit is set.

If *ex* is set the crystal is active during sleep mode. When *dc* bit is set it disables the clock output

2. Frequency Setting Command

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0	POR
	1	0	1	0	f11	f10	f9	f8	f7	f6	f5	f4	f3	f2	f1	f0	A680h

The 12-bit parameter of the *Frequency Setting Command <f11 : f0>* has the value F. The value F should be in the range of 96 and 3903. When F is out of range, the previous value is kept. The synthesizer center frequency f_0 can be calculated as:

$$f_0 = 10\ MHz * C1 * (C2 + F/4000)$$

The constants C1 and C2 are determined by the selected band as:

Band [MHz]	C1	C2
315	1	31
433	1	43
868	2	43
915	3	30

3. Receiver Setting Command

bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0	POR
	1	1	0	0	0	0	0	0	d1	d0	g1	g0	r2	r1	r0	en	C0C1h

Bits 7-6 select the VDI (valid data indicator) signal:

d1	d0	VDI output
0	0	Digital RSSI Out (DRSSI)
0	1	Data Quality Detector Output (DQD)
1	0	Clock recovery lock
1	1	DRSSI && DQD

Bits 5-4 LNA gain set:

g1	g0	G_{LNA} (dB relative to max. G)
0	0	0
0	1	-14
1	0	-6
1	1	-20

Bits 3-1 control the threshold of the RSSI detector:

r2	r1	r0	$RSSI_{setth}$ [dBm]
0	0	0	-103
0	0	1	-97
0	1	0	-91
0	1	1	-85
1	0	0	-79
1	0	1	-73
1	1	0	Reserved
1	1	1	Reserved

The RSSI threshold depends on the LNA gain, the real RSSI threshold can be calculated:

$$RSSI_{th} = RSSI_{setth} + G_{LNA}$$

Bit 0 (*en*) enables the whole receiver chain when set. Enable/disable of the wake-up timer and the low battery detector are not affected by this setting.

Note: Clock tail is not generated when the crystal oscillator is controlled by *en* bit.

4. Wake-Up Timer Command

bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0	POR
	1	1	1	r4	r3	r2	r1	r0	m7	m6	m5	m4	m3	m2	m1	m0	E196h

The wake-up time period can be calculated by M <*m7* : *m0*> and R <*r4* : *r0*>:

$T_{wake-up} = M * 2^R ms$

Software reset: Sending FF00h command to the chip triggers software reset. For more details see the *Reset modes* section.

5. Low Duty-Cycle Command

bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0	POR
	1	1	0	0	1	1	0	0	d6	d5	d4	d3	d2	d1	d0	en	CC0Eh

With this command Low Duty-Cycle operation can be set in order to decrease the average power consumption.

The time cycle is determined by the *Wake-Up Timer Command*.

The Duty-Cycle is calculated by D <*d6* : *d0*> and M. (M is parameter in a *Wake-Up Timer Command*.)

D.C.= (D * 2 +1) / M *100%

6. Low Battery Detector and Microcontroller Clock Divider Command

bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0	POR
	1	1	0	0	0	0	1	0	d2	d1	d0	t4	t3	t2	t1	t0	C200h

The 5-bit value T of *t4-t0* determines the threshold voltage of the threshold voltage V_{lb} of the detector:

V_{lb}= 2.25 V + T * 0.1 V

Clock divider configuration:

d2	d1	d0	Clock Output Frequency [MHz]
0	0	0	1
0	0	1	1.25
0	1	0	1.66
0	1	1	2
1	0	0	2.5
1	0	1	3.33
1	1	0	5
1	1	1	10

7. AFC Command

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0	POR
	1	1	0	0	0	1	1	0	a1	a0	rl1	rl0	st	fi	oe	en	C6F7h

Bit 0 (*en)* enables the calculation of the offset frequency by the AFC circuit (it allows the addition of the content of the output register to the frequency control word of the PLL).

Bit 1 (*oe*) when set, enables the output (frequency offset) register

Bit 2 (*fi*) when set, switches the circuit to high accuracy (fine) mode. In this case the processing time is about four times longer, but the measurement uncertainty is less than half.

Bit 3 (*st*) strobe edge, when *st* goes to high, the actual latest calculated frequency error is stored into the output registers of the AFC block.

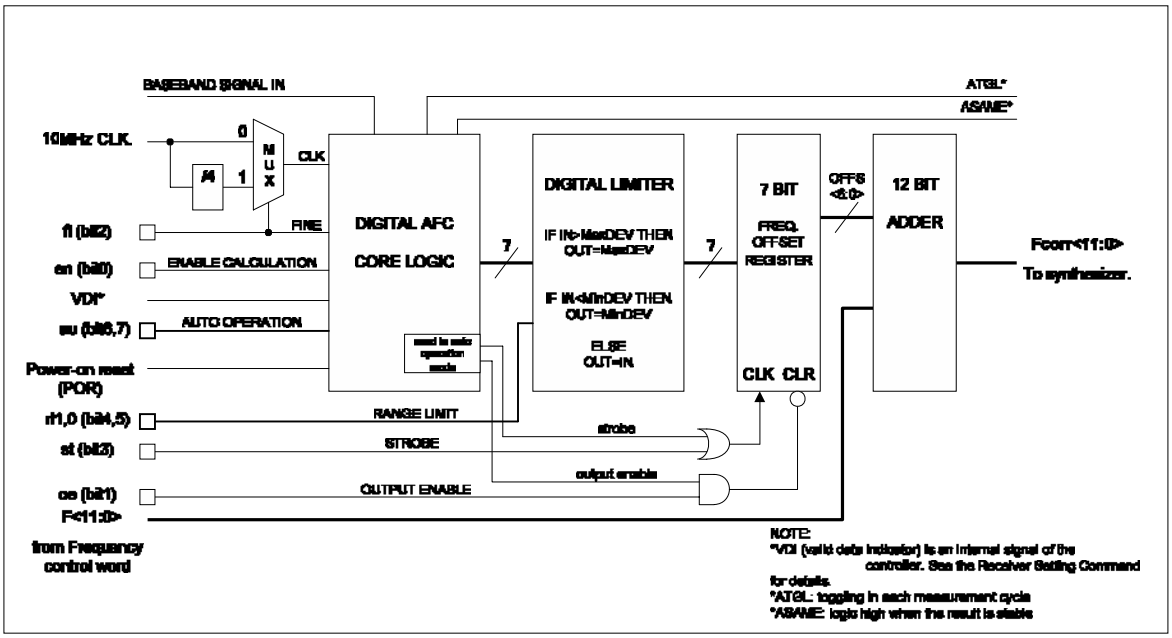
Bit 4-5 (*rl0*, *rl1*) range limit: Limits the value of the frequency offset register to the following values:

rl1	rl0	Max dev [f_{res}]
0	0	No restriction
0	1	+15/-16
1	0	+7/-8
1	1	+3/-4

f_{res}:
315, 433MHz bands: 2.5kHz
868MHz band: 5kHz
915MHz band: 7.5kHz

Bit 6-7 (*a0*, *a1*) Automatic operation mode selector:

a1	a0	Automatic operation mode
0	0	Auto mode off (Strobe is controlled by microcontroller)
0	1	Runs only once after each power-up
1	0	Drop the f_{offset} value when the VDI signal is low
1	1	Keep the f_{offset} value independently from the state of the VDI signal



In automatic operation mode (no strobe signal is needed from the microcontroller to update the output offset register), the AFC circuit is automatically enabled when VDI indicates a potential incoming signal during the whole measurement cycle and the circuit measures the same result in two subsequent cycles.

There are three operation modes, example from the possible application:

1, (*a1*=0, *a0*=1) The circuit measures the frequency offset only once after power up. This way, the extended TX/RX maximum distance can be achieved. Possible usage: In the final application when the user is inserted the battery the circuit measures and compensate the frequency offset caused by the crystal tolerances. This method enables to use cheaper quartz in the application and provide quite good protection against locking in an interferer.

2a, (*a1*=1, *a0*=0) The circuit measures automatically the frequency offset during an initial low data rate pattern –easier to receive- (i.e.: 00110011) of the package and change the receiving frequency according that. The further part of the package can be received by the corrected frequency settings.

2b, (*a1*=1, *a0*=0) The transmitter must transmit the first part of the packet with a step higher deviation and later there is a possibility to reduce it.

In both cases (*2a* and *2b*) when the VDI indicates poor receiving conditions (VDI goes low) the output register is automatically cleared. It's suggested to use when one receiver receives signal from more than one transmitter.

3, (a1=1, a0=1) It is similar to the 2a and 2b modes, but 3 is suggested to use when a receiver operates with only one transmitter. After a complete measuring cycle, the measured value is held independently of the sate of VDI signal.

8. Data Filter Command

bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0	POR
	1	1	0	0	0	1	0	0	al	ml	1	s1	s0	f2	f1	f0	C42Ch

Bit 7 <al>: Clock recovery (CR) auto lock control if set.

It means that the CR start in fast mode after locking it automatically switches to slow mode.

Bit 6 <ml>: Clock recovery lock control

1: fast mode, fast attack and fast release

0: slow mode, slow attack and slow release

Using the slower one requires more accurate bit timing (see Data Rate Command).

Bit 3-4 <s0 : s1>: Select the type of the data filter:

s1	s0	Filter Type
0	0	OOK to filter
0	1	Digital filter
1	0	Reserved
1	1	Analog RC filter

OOK to filter: the analog RSSI signal is used as received data. The DRSSI threshold level is used for slicing.

Digital: this is a digital realization of an analog RC filter followed by a comparator with hysteresis. The time constant is automatically adjusted to the bit rate defined by the Data Rate Command.

Analog RC filter: The demodulator output is fed to pin 7 over a 10 kOhm resistor. The filter cut-off frequency is set by the external capacitor connected to this pin and VSS.

The table shows the optimal filter capacitor values for different data rates:

1.2 kbps	2.4 kbps	4.8 kbps	9.6 kbps	19.2 kbps	38.4 kbps	57.6 kbps	115.2 kbps	256 kbps
12 nF	8.2 nF	6.8 nF	3.3 nF	1.5 nF	680 pF	270 pF	150 pF	100 pF

Note: If analog RC filter is selected the internal clock recovery circuit and the FIFO cannot be used.

Bit 0-2 <f0 : f2>: DQD threshold parameter.

Note: To let the DQD report "good signal quality" the threshold parameter should be less than 4 in the case when the bitrate is close to the deviation. At higher deviation/bitrate settings higher threshold parameter can report "good signal quality" as well.

9. Data Rate Command

bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0	POR
	1	1	0	0	1	0	0	0	cs	r6	r5	r4	r3	r2	r1	r0	C823h

The expected bit rate of the received data stream is determined by the 7-bit value R (bits *r6* to *r0*) and the 1 bit *cs*.

BR = 10 MHz / 29 / (R+1) / (*1* + *cs**7)

In the receiver set R according the next function:

R= (10 MHz / 29 / (*1* + *cs**7)/ BR) – 1

Apart from setting custom values, the standard bit rates from 600 bps to 115.2 kbps can be approximated with small error.

Data rate accuracy requirements:

Clock recovery in slow mode: $\Delta BR/BR < 1/(29*N_{bit})$ Clock recovery in fast mode: $\Delta BR/BR<3/(29*N_{bit})$

BR is the bit rate set in the receiver and ΔBR is bit rate difference between the transmitter and the receiver. N_{bit} is the maximal number of consecutive ones or zeros in the data stream. It is recommended for long data packets to include enough 1/0 and 0/1 transitions, and be careful to use the same division ratio in the receiver and in the transmitter.

ΔBR is a theoretical limit for the clock recovery circuit. Clock recovery will not work above this limit. The clock recovery circuit will always operate below this limit independently from process, temperature, or V_{dd} condition.

Supposing a maximum length of consecutive zeros or ones in the data stream is less than 5 bits, the necessary relative accuracy is 0.68% in slow mode and 2.1% in fast mode.

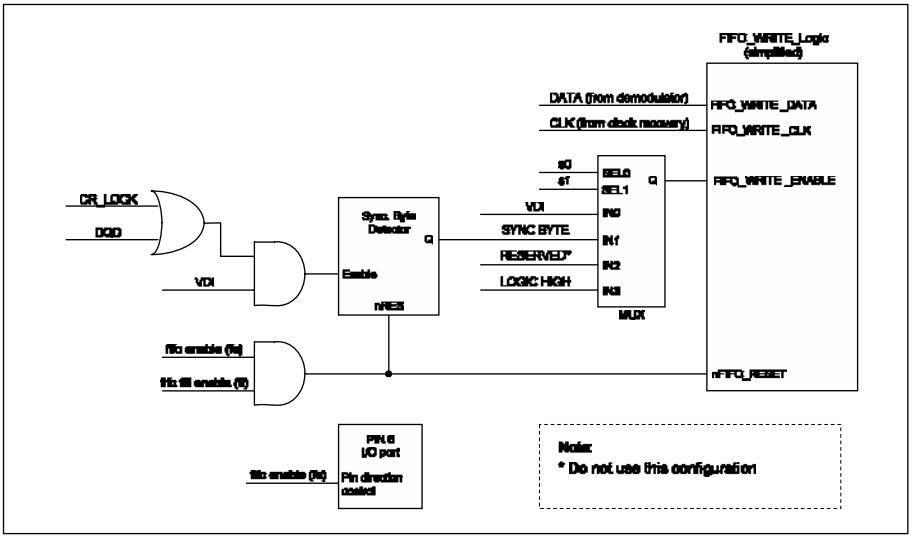
10. Output and FIFO Mode Command

bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0	POR
	1	1	0	0	1	1	1	0	f3	f2	f1	f0	s1	s0	ff	fe	CE85h

Bit 4-7 <*f3* : *f0*>: FIFO IT level. The FIFO generates IT when number of the received data bits reaches this level.

Bit 2-3 <*s1* : *s0*>: Set the input of the FIFO fill start condition:

s1	s0	FIFO fill start condition
0	0	VDI
0	1	Sync Word
1	0	Reserved
1	1	Always



Note: VDI (Valid Data Indicator) see further details in *Receiver Control Word*, Synchron word in microcontroller mode is 2DD4h.

Bit 1: <*ff*> Enables FIFO fill after synchron word reception. FIFO fill stops when this bit is cleared.

Bit 0: <*fe*> Enables the 16bit deep FIFO mode. To clear the FIFO's counter and content, it has to be set zero.

Note: To restart the synchron word reception, bit 1 should be cleared and set. This action will initialize the FIFO and clear its content.

Bit 0 modifies the function of pin 6 and pin 7. Pin 6 (nFFS) will become input if *fe* is set to 1. If the chip is used in FIFO mode, do not allow this to be a floating input.

11. Reset Mode Command

bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0	POR
	1	1	0	1	1	0	1	0	0	0	0	0	0	0	0	dr	DA00h

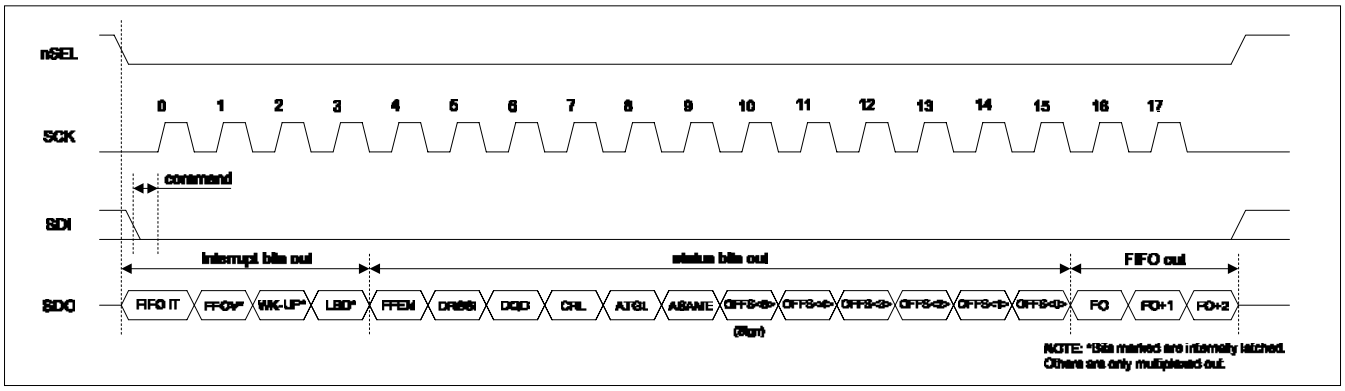
Bit 0 (*dr*): Disables the highly sensitive RESET mode. If this bit is cleared, a 600 mV glitch in the power supply may cause a system reset. For more detailed description see the *Reset modes* section.

12. Status Read Command

bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0	POR
	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	- -

The read command starts with a zero, whereas all other control commands start with a one. Therefore, after receiving the first bit of the control command the RFM01 identifies it as a read command. So as the first bit of the command is received, the receiver starts to clock out the status bits on the SDO output as follows:

Status Register Read Sequence with FIFO Read Example



It is possible to read out the content of the FIFO after the reading of the status bits. The command can be aborted after any read bits by rising edge of the select signal.

Note: The FIFO IT bit behaves like a status bit, but generates nIRQ pulse if active. To check whether there is a sufficient amount of data in the FIFO, the SDO output can be tested. In extreme speed critical applications, it can be useful to read only the first four bits (*FIFO IT - LBD*) to clear the FFOV, WK-UP, and LBD bits. During the FIFO access the f_{SCK} cannot be higher than f_{ref} /4, where f_{ref} is the crystal oscillator frequency. If the FIFO is read in this mode the nFFS input must be connected to logic high level.

Definitions of the bits in the above timing diagram:

FIFO IT	Number of the data bits in the FIFO is reached the preprogrammed limit
FFOV	FIFO overflow
WK-UP	Wake-up timer overflow
LBD	Low battery detect, the power supply voltage is below the preprogrammed limit
FFEM	FIFO is empty
DRSSI	The strength of the incoming signal is above the preprogrammed limit
DQD	Data Quality Detector detected a good quality signal
CRL	Clock recovery lock
ATGL	Toggling in each AFC cycle
ASAME	AFC stabilized (measured twice the same offset value)
OFFS6, 4-0	Offset value to be added to the value of the Frequency control word

FIFO Buffered Data Read

In this operating mode, incoming data are clocked into a 16 bit FIFO buffer. The receiver starts to fill up the FIFO when the Valid Data Indicator (VDI) bit and/or the synchron word recognition circuit indicates potentially real incoming data. This prevents the FIFO from being filled with noise and overloading the external microcontroller.

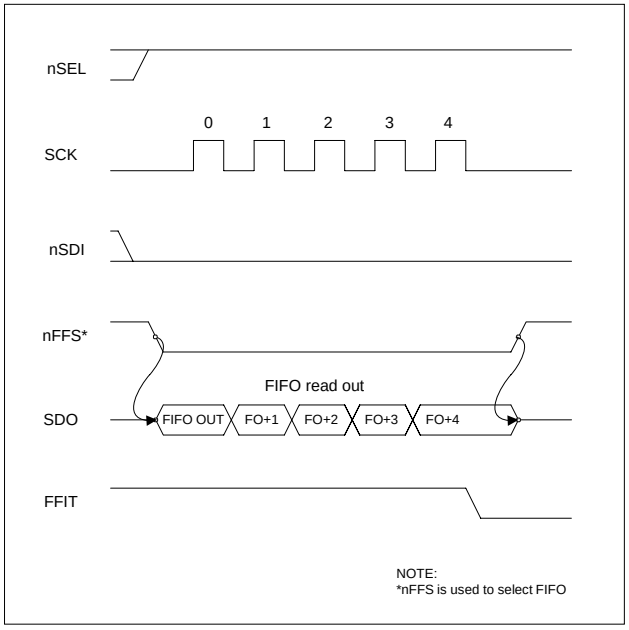
For further details see the *Receiver Setting Command* and the *Output and FIFO Command*.

Polling Mode:

The nFFS signal selects the buffer directly and its content could be clocked out through pin SDO by SCK. Set the FIFO IT level to 1. In this case, as long as FFIT indicates received bits in the FIFO, the controller may continue to take the bits away. When FFIT goes low, no more bits need to be taken. An SPI read command is also available.

Interrupt Controlled Mode:

The user can define the FIFO level (the number of received bits) which will generate the nFFIT when exceeded. The status bits report the changed FIFO status in this case.



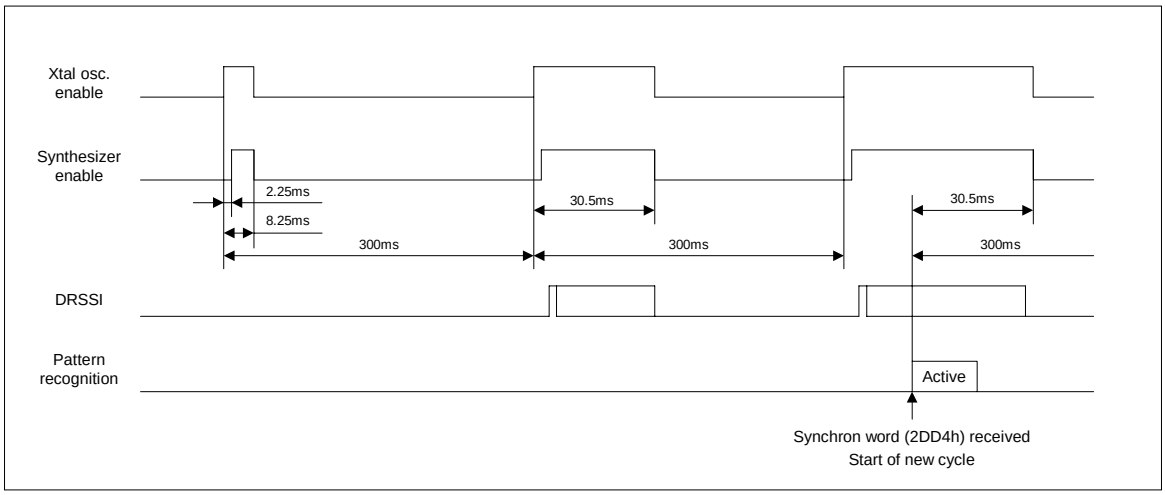
During FIFO access the f_{SCK} cannot be higher than $f_{ref}/4$, where f_{ref} is the crystal oscillator frequency.

Low Power Duty-Cycle Operation (LPDM)

To use this mode, pin 8 must be connected to VDD. The logic value of pin 8 defines whether the receiver works in *Low Power Duty-Cycle Mode* (LPDM) or not. If the value is high (VDD detected), the chip will wake up in every 300 ms. If the value is low (GND detected), then the chip is continually ON (active). The chip uses the internal wake-up timer and counter for timing the on/off process. This method reduces the overall current consumption, which should permit approximately 6 months operation from a 1500 mAh battery.

Low Power Duty-Cycle Internal Operations and Timings (Wake-up on Radio)

The wake-up timer event switches on the crystal oscillator, the internal logic waits about 2.25ms. When the oscillator is stable the controller switches on the synthesizer as well. The receiver monitors the incoming signal strength during this "ON" state of LPDM. If in the next 6ms the incoming signal strength is above the defined limit (-103dBm if FCS0=0 or -97dBm if FCS0=1), the synthesizer remains switched on for 30.5ms, otherwise it switches itself off after the 6ms operation time. The period time is about 300ms.



Note 1: Every detected synchron word restarts the timer, which controls the 'ON' state of the receiver.

Note 2: If the internal *Pattern Recognition* block is active (decoding the synchron word), then the internal logic does not switch the synthesizer off until the incoming data is fully processed.

RX-TX ALIGNMENT PROCEDURES

RX-TX frequency offset can be caused only by the differences in the actual reference frequency. To minimize these errors it is suggested to use the same crystal type and the same PCB layout for the crystal placement on the RX and TX PCBs.

To verify the possible RX-TX offset it is suggested to measure the CLK output of both chips with a high level of accuracy. Do not measure the output at the XTL pin since the measurement process itself will change the reference frequency. Since the carrier frequencies are derived from the reference frequency, having identical reference frequencies and nominal frequency settings at the TX and RX side there should be no offset if the CLK signals have identical frequencies.

It is possible to monitor the actual RX-TX offset using the AFC status report included in the status byte of the receiver. By reading out the status byte from the receiver, the actual measured offset frequency will be reported. In order to get accurate values the AFC has to be disabled during the read by clearing the "en" bit in the AFC Control Command (bit 0).

CRYSTAL SELECTION GUIDELINES

The crystal oscillator of the RFM01 requires a 10 MHz parallel mode crystal. The circuit contains an integrated load capacitor in order to minimize the external component count. The internal load capacitance value is programmable from 8.5 pF to 16 pF in 0.5 pF steps. With appropriate PCB layout, the total load capacitance value can be 10 pF to 20 pF so a variety of crystal types can be used.

When the total load capacitance is not more than 20 pF and a worst case 7 pF shunt capacitance (C_0) value is expected for the crystal, the oscillator is able to start up with any crystal having less than 300 ohms ESR (equivalent series loss resistance). However, lower C_0 and ESR values guarantee faster oscillator startup.

The crystal frequency is used as the reference of the PLL, which generates the local oscillator frequency (f_{LO}). Therefore, f_{LO} is directly proportional to the crystal frequency. The accuracy requirements for production tolerance, temperature drift and aging can thus be determined from the maximum allowable local oscillator frequency error.

Maximum XTAL Tolerances Including Temperature and Aging [ppm]

Bit Rate: 2.4kbps

	Transmitter Deviation [+/- kHz]						
	30	**60**	**90**	**120**	**150**	**180**	**210**
315 MHz	30	75	100	100	100	100	100
433 MHz	20	50	75	100	100	100	100
868 MHz	10	25	40	60	75	100	100
915 MHz	10	25	40	50	75	75	100

Bit Rate: 9.6kbps

	Transmitter Deviation [+/- kHz]						
	30	**60**	**90**	**120**	**150**	**180**	**210**
315 MHz	25	70	100	100	100	100	100
433 MHz	15	50	75	100	100	100	100
868 MHz	8	25	40	60	75	75	100
915 MHz	8	25	40	50	70	75	100

Bit Rate: 38.3kbps

	Transmitter Deviation [+/- kHz]						
	30	**60**	**90**	**120**	**150**	**180**	**210**
315 MHz	don't use	30	75	100	100	100	100
433 MHz	don't use	20	50	75	100	100	100
868 MHz	don't use	10	30	40	60	75	100
915 MHz	don't use	10	25	40	60	75	75

Whenever a low frequency error is essential for the application, it is possible to "pull" the crystal to the accurate frequency by changing the load capacitor value. The widest pulling range can be achieved if the nominal required load capacitance of the crystal is in the "midrange", for example 16 pF. The "pull-ability" of the crystal is defined by its motional capacitance and C_0.

The on chip AFC is capable to correct TX/RX carrier offsets as much as 80% of the deviation of the received FSK modulated signal.

Note: There may be other requirements for the TX carrier accuracy with regards to the requirements as defined by standards and/or channel separations.

RESET MODES

The chip will enter into reset mode if any of the following conditions are met:

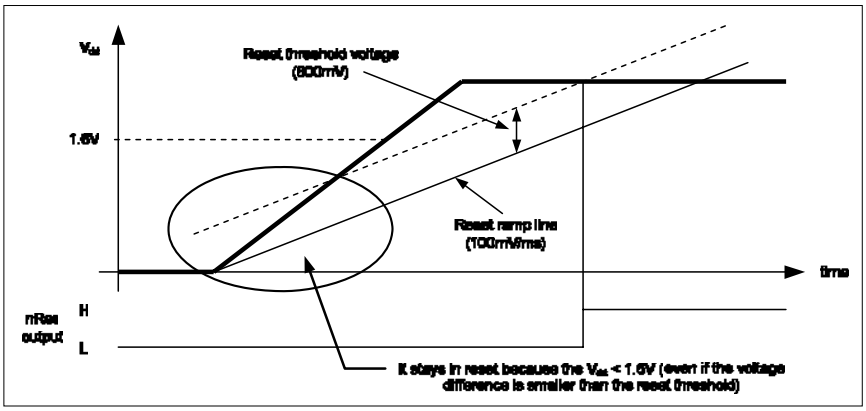
- Power-on reset: During a power up sequence until the V_{dd} has reached the correct level and stabilized
- Power glitch reset: Transients present on the V_{dd} line
- Software reset: Special control command received by the chip

Power-on reset

After power up the supply voltage starts to rise from 0V. The reset block has an internal ramping voltage reference (reset-ramp signal), which is rising at 100mV/ms (typical) rate. The chip remains in reset state while the voltage difference between the actual V_{dd} and the internal reset-ramp signal is higher than the reset threshold voltage, which is 600 mV (typical). As long as the V_{dd} voltage is less than 1.6V (typical) the chip stays in reset mode regardless the voltage difference between the V_{dd} and the internal ramp signal.

The reset event can last up to 150ms supposing that the V_{dd} reaches 90% its final value within 1ms. During this period the chip does not accept control commands via the serial control interface.

Power-on reset example:



Power glitch reset

The internal reset block has two basic mode of operation: normal and sensitive reset. The default mode is sensitive, which can be changed by the appropriate control command (see *Related control commands* at the end of this section). In normal mode the power glitch detection circuit is disabled.

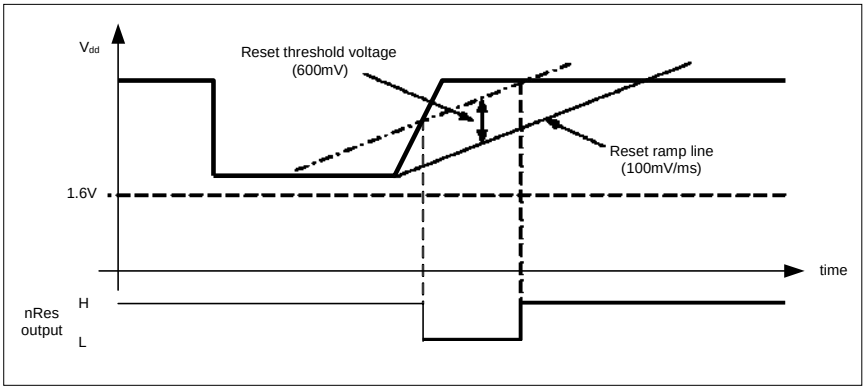
There can be spikes or glitches on the V_{dd} line if the supply filtering is not satisfactory or the internal resistance of the power supply is too high. In such cases if the sensitive reset is enabled an (unwanted) reset will be generated if the positive going edge of the V_{dd} has a rising rate greater than 100mV/ms and the voltage difference between the internal ramp signal and the V_{dd} reaches the reset threshold voltage (600 mV). Typical case when the battery is weak and due to its increased internal resistance a sudden decrease of the current consumption (for example turning off the power amplifier) might lead to an increase in supply voltage. If for some reason the sensitive reset cannot be disabled step-by-step decrease of the current consumption (by turning off the different stages one by one) can help to avoid this problem.

Any negative change in the supply voltage will not cause reset event unless the V_{dd} level reaches the reset threshold voltage (250mV in normal mode, 1.6V in sensitive reset mode).

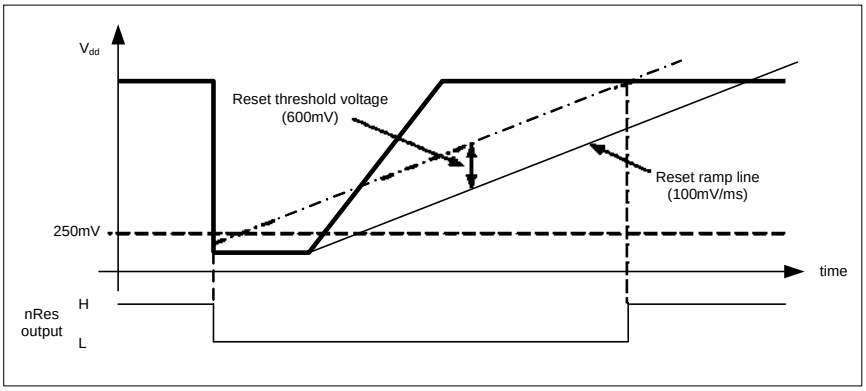
If the sensitive mode is disabled and the power supply turned off the V_{dd} must drop below 250mV in order to trigger a power-on reset event when the supply voltage is turned back on. If the decoupling capacitors keep their charges for a long time it could happen that no reset will be generated upon power-up because the power glitch detector circuit is disabled.

Note that the reset event reinitializes the internal registers, so the sensitive mode will be enabled again.

Sensitive Reset Enabled, Ripple on V_{dd}:



Sensitive reset disabled:



Software reset

Software reset can be issued by sending the appropriate control command (described at the end of the section) to the chip. The result of the command is the same as if power-on reset was occurred. When the nRES pin connected to the reset pin of the microcontroller, using the software reset command may cause unexpected problems.

V_{dd} line filtering

During the reset event (caused by power-on, fast positive spike on the supply line or software reset command) it is very important to keep the V_{dd} line as smooth as possible. Noise or periodic disturbing signal superimposed the supply voltage may prevent the part getting out from reset state. To avoid this phenomenon use adequate filtering on the power supply line to keep the level of the disturbing signal below $10mV_{p-p}$ in the DC – 50kHz range for 200ms from V_{dd} ramp start.. Typical example when a switch-mode regulator is used to supply the radio, switching noise may be present on the V_{dd} line. Follow the manufacturer's recommendations how to decrease the ripple of the regulator IC and/or how to shift the switching frequency.

Related control commands

"Reset Mode Command"

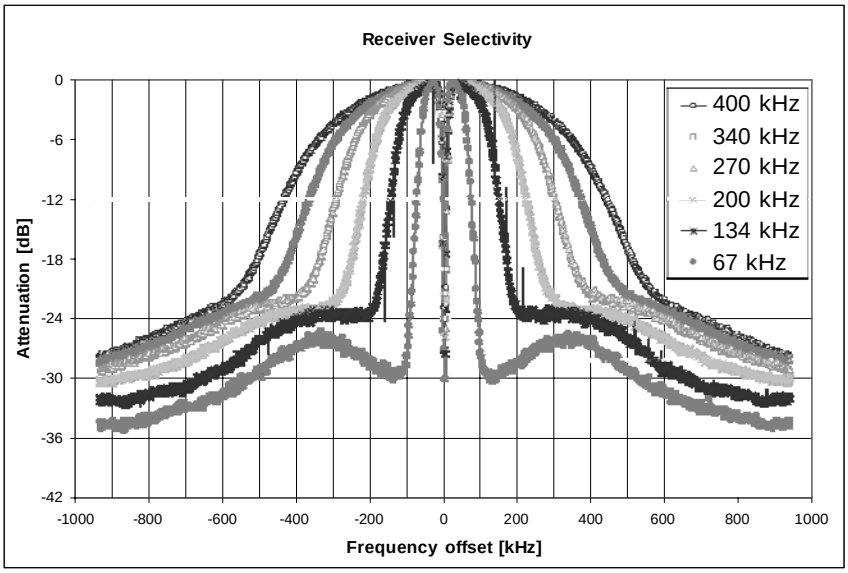
Setting bit<0> to high will change the reset mode to normal from the default sensitive.

"SW Reset Command"

Issuing FF00h command will trigger software reset. See the *Wake-up Timer Command*.

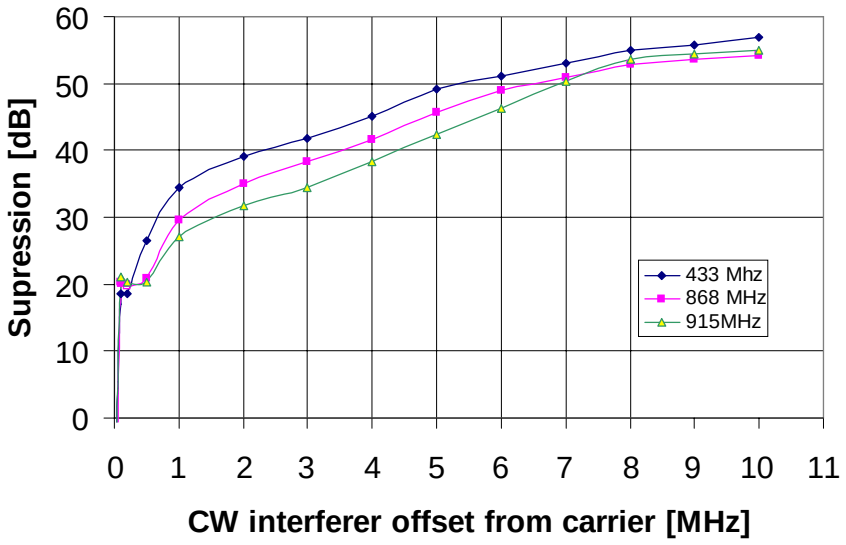
MEASUREMENT RESULTS

Receiver Selectivity at Different Baseband Filter Settings



TYPICAL PERFORMANCE CHARACTERISTICS

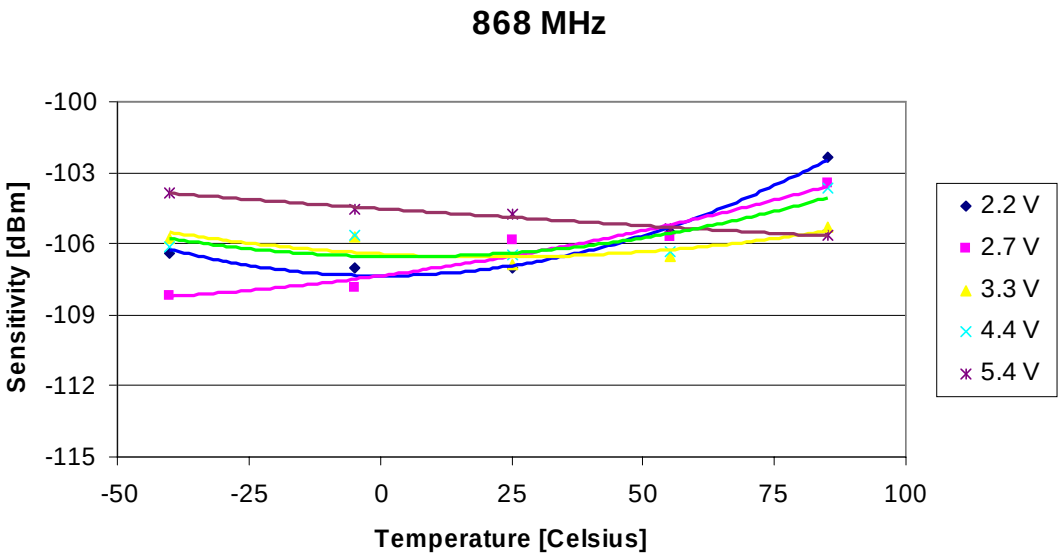
Channel Selectivity and Blocking



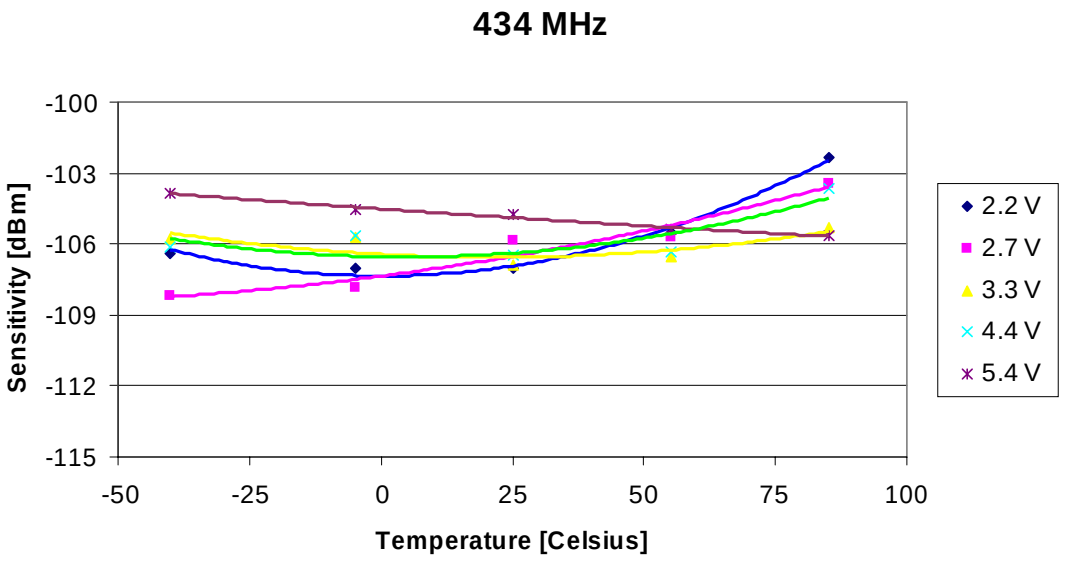
Note:

- LNA gain maximum, filter bandwidth 67 kHz, data rate 9.6 kbps, AFC switched off, FSK deviation +/- 45 kHz, V_{dd} 3V,
- Measured in compliant with ETSI Standard EN 300 220-1 v2.1.1 (2006-01 Final Draft), section 9

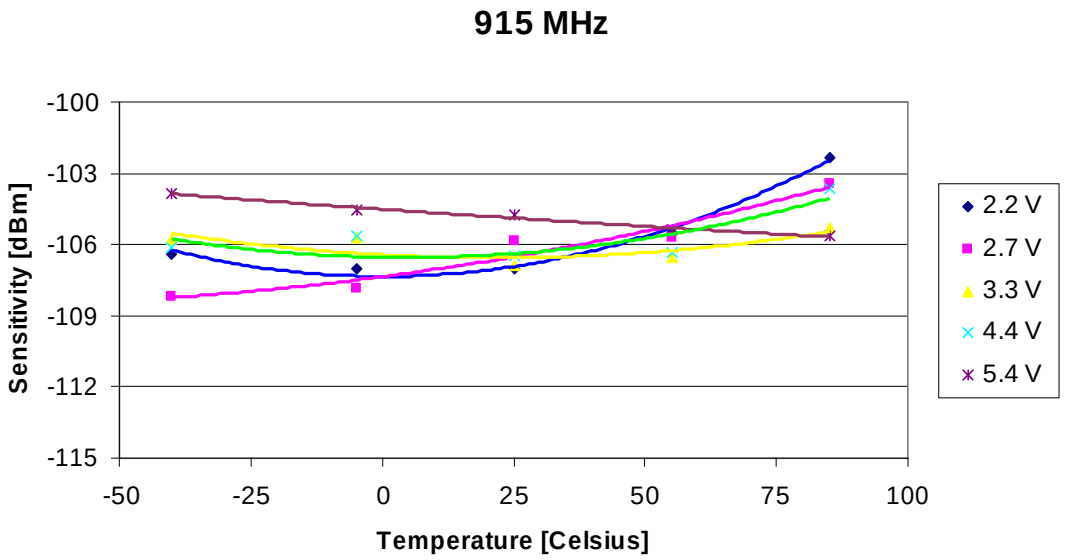
Sensitivity over Ambient Temperature (868 MHz, 9.6 kbps, dfsk: 45 kHz, BW: 67 kHz)



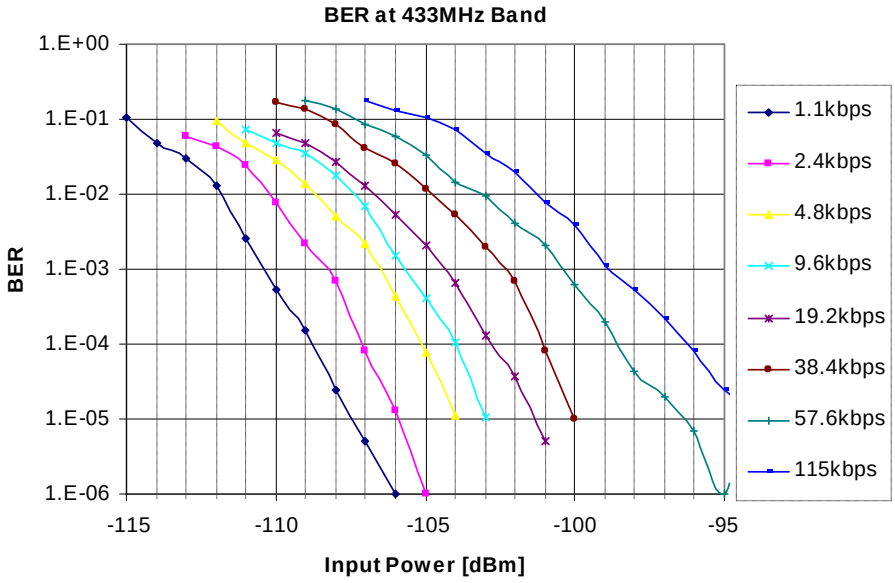
Sensitivity over Ambient Temperature (434 MHz, 9.6 kbps, dfsk: 45 kHz, BW: 67 kHz)

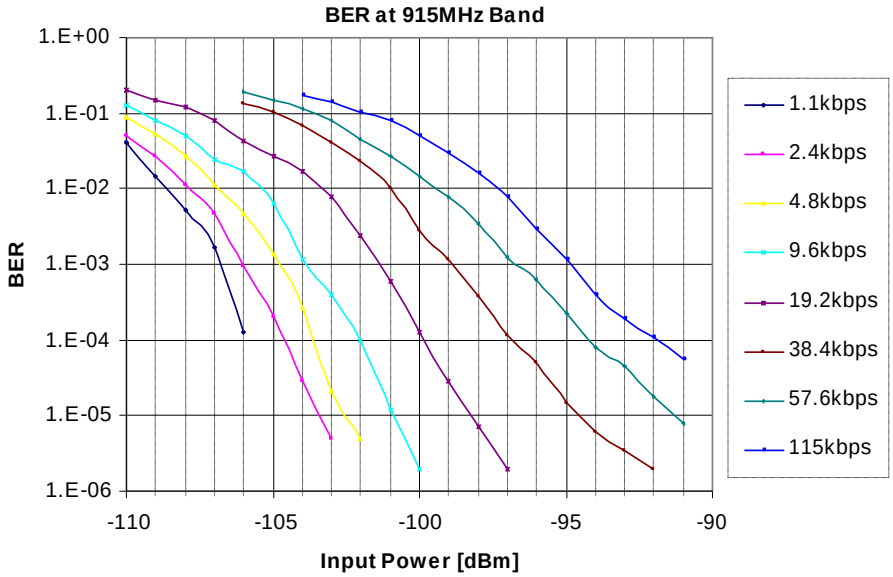


Sensitivity over Ambient Temperature (915 MHz, 9.6 kbps, dfsk: 45 kHz, BW: 67 kHz)



BER Measurement Results

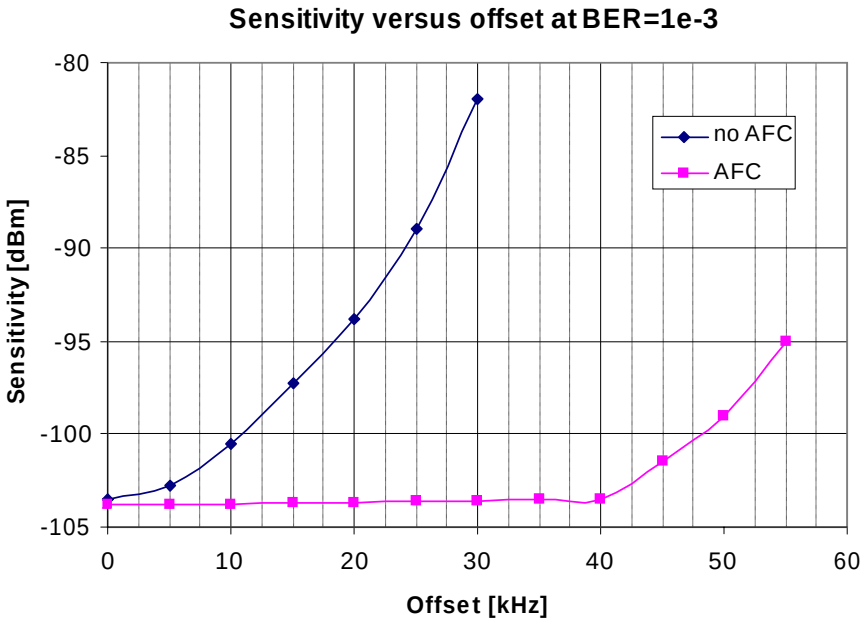




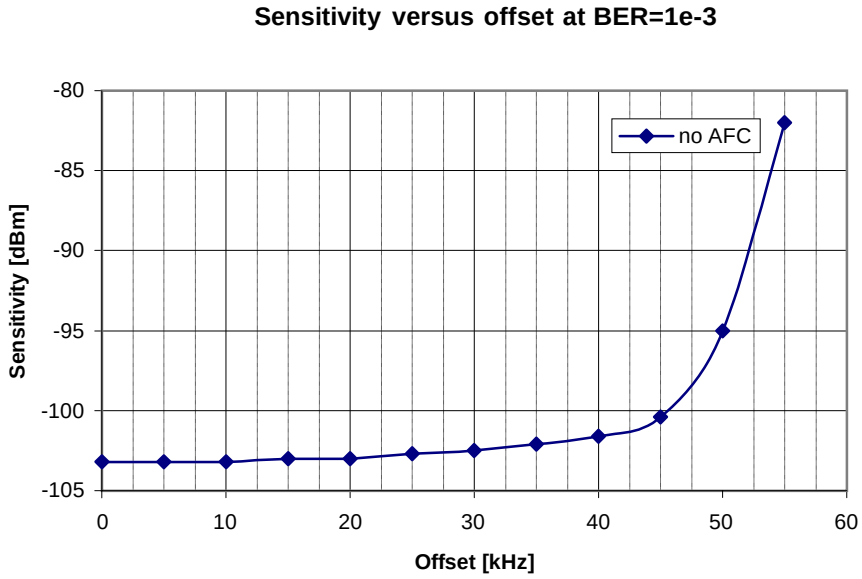
1.134 kbps	2.4 kbps	4.8 kbps	9.6 kbps	19.2 kbps	38.4 kbps	57.6 kbps	115 kbps
BW=67 kHz δf_{FSK} =30 kHz	BW=67 kHz δf_{FSK} =30 kHz	BW=67 kHz δf_{FSK} =30 kHz	BW=67 kHz δf_{FSK} =45 kHz	BW=67 kHz δf_{FSK} =45 kHz	BW=134 kHz δf_{FSK} =90 kHz	BW=134 kHz δf_{FSK} =90 kHz	BW=200 kHz δf_{FSK} =120 kHz

The table shows the optimal BW and δf_{FSK} selection for different data rates. Recommended only when using accurate crystal (20ppm or better).

Frequency Offset Effecter Sensitivity Degradation



BR=9.6 kbps, BER=10^{-3} , BW=67 kHz, δf_{FSK} =60 kHz

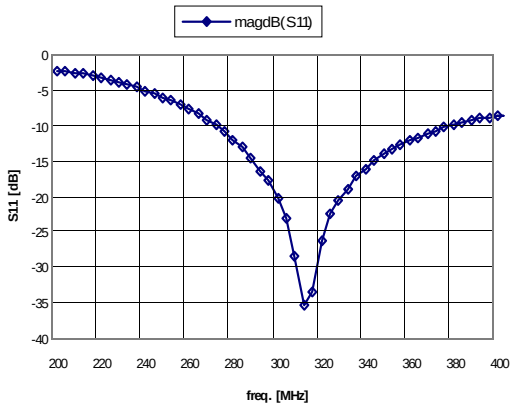


BR=9.6 kbps, BER=10^{-3} , BW=134 kHz, δf_{FSK} =60 kHz

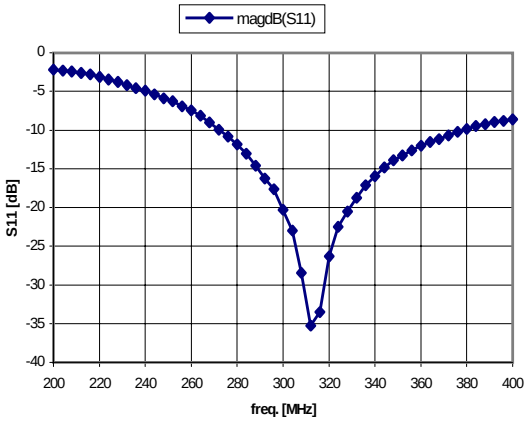
Input impedance

Measured input return loss on the demo boards with suggested matching circuit

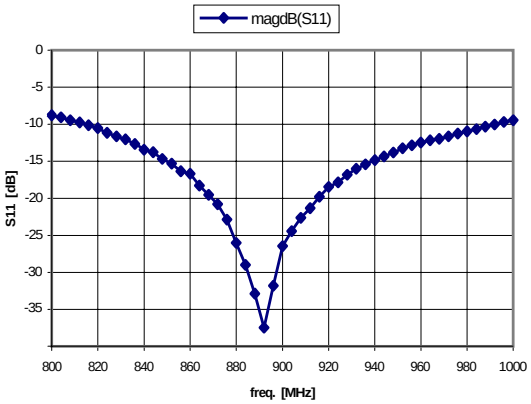
315 MHz Matching to 50 Ohm



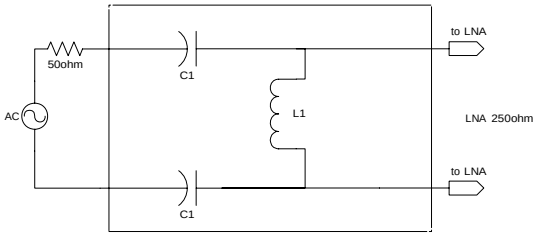
433 MHz Matching to 50 Ohm



868 and 915 MHz Matching to 50 Ohm



Input Matching circuit

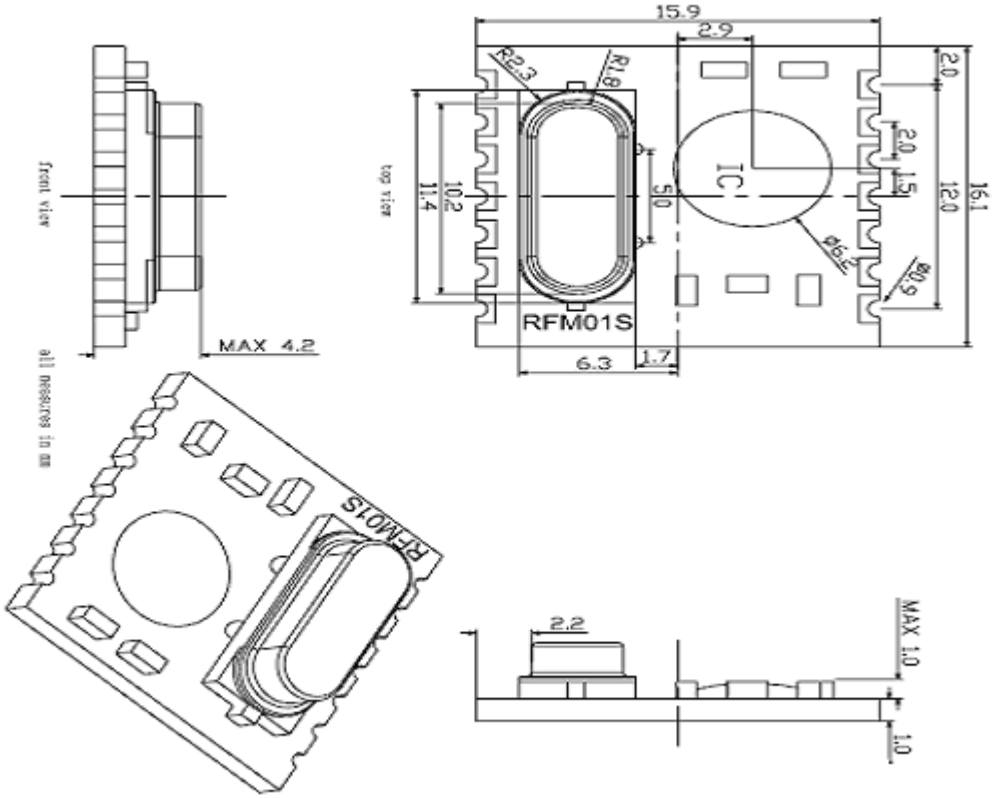


Frequency [MHz]	L1 [nH]	C1 [pF]
915	15	3
868	15	3
433	36	7
315	56	9

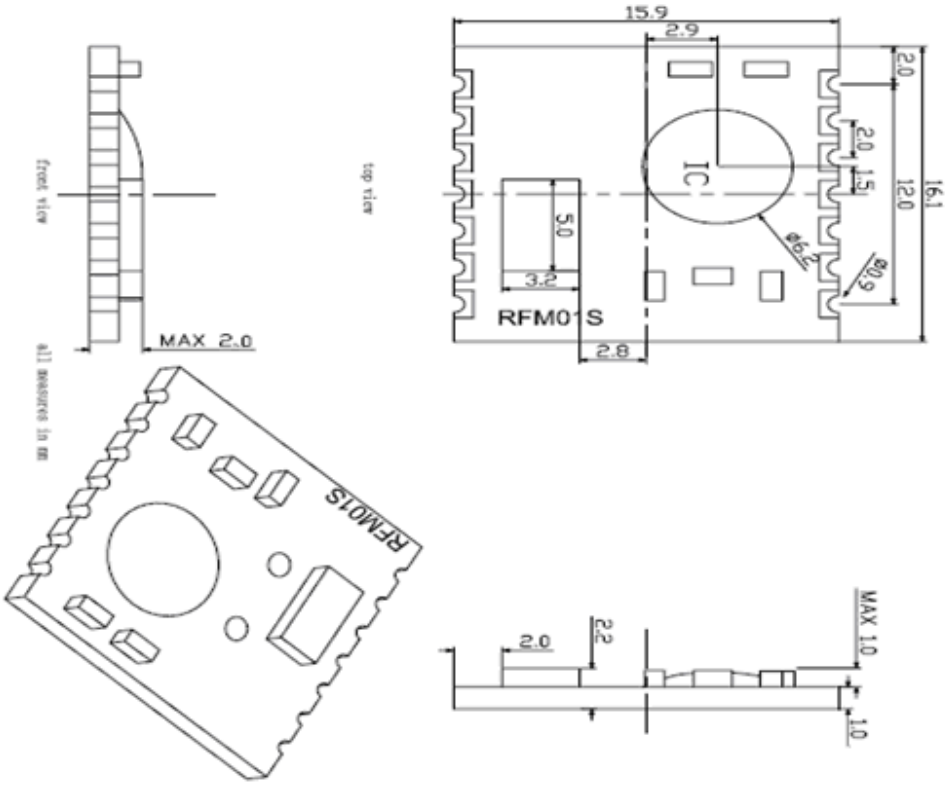
PACKAGE INFORMATION

（units in mm）

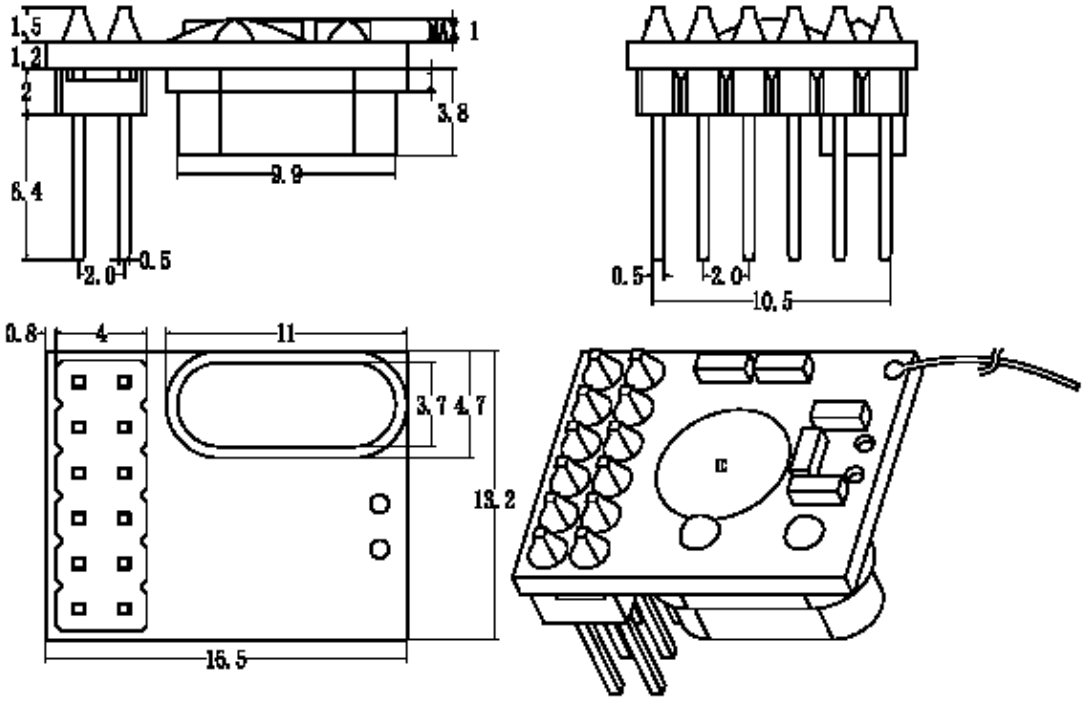
SMD PACKAGE（S1）



SMD PACKAGE（S2）



DIP PACKAGE（D）



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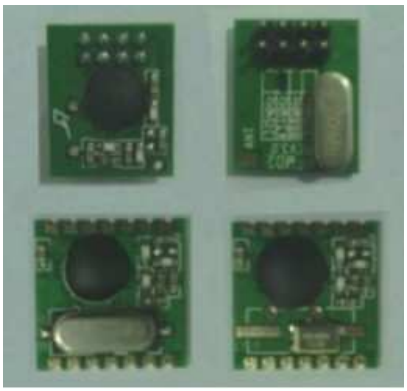
RFM02 Universal ISM Band FSK Transmitter

RFM02

DESCRIPTION



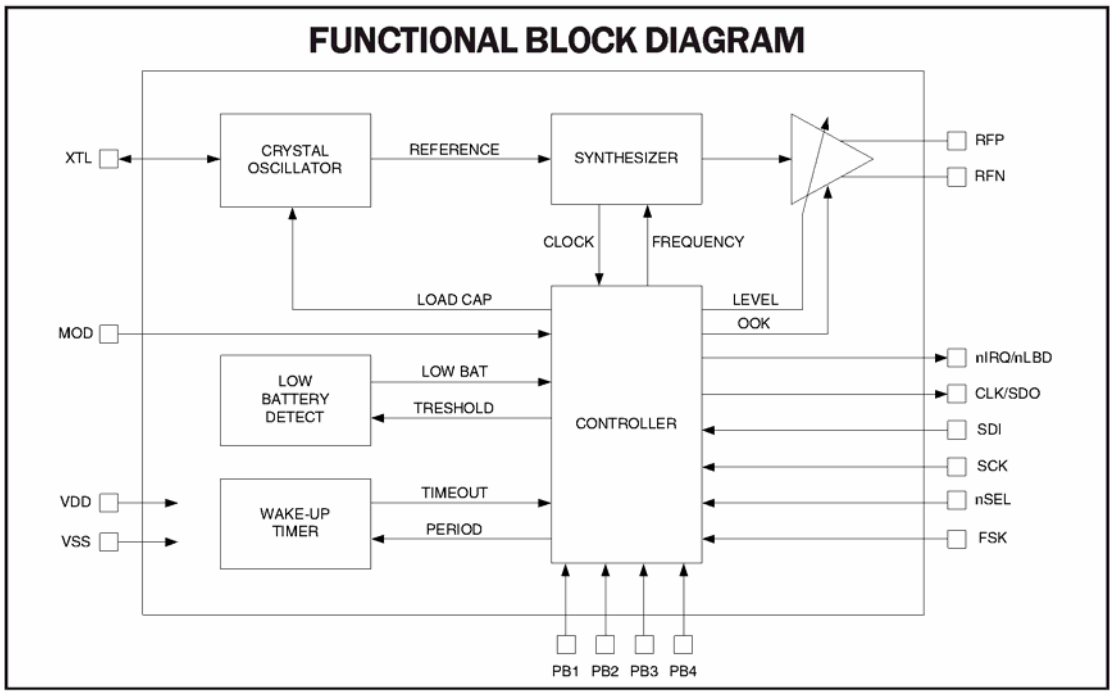
Hope's RFM02 is a single chip, low power, multi-channel FSK transmitter designed for use in applications requiring FCC or ETSI conformance for unlicensed use in the 433, 868, and 915 MHz bands. Used in conjunction with RF01, Hope's FSK receiver, the RFM02 transmitter produces a flexible, low cost, and highly integrated solution that does not require production alignments. All required RF functions are integrated. Only an external crystal and bypass filtering are needed for operation. The RFM02 offering a higher output power and an improved phase noise characteristic.

The RFM02 features a completely integrated PLL for easy RF design, and its rapid settling time allows for fast frequency hopping, bypassing multipath fading and interference to achieve robust wireless links. In addition, highly stable and accurate FSK modulation is accomplished by direct closed-loop modulation with bit rates up to 115.2 kbps. The PLL's high resolution allows the use of multiple channels in any of the bands.

The integrated power amplifier of the transmitter has an open-collector differential output that directly drive a loop antenna with programmable output level. No additional matching network is required. An automatic antenna tuning circuit is built in to avoid costly trimming procedures and de-tuning due to the "hand effect".

For low-power applications, the device supports automatic activation from sleep mode. Active mode can be initiated by several wake-up events (on-chip timer timeout, low supply voltage detection).

FUNCTIONAL BLOCK DIAGRAM



FEATURES

- Fully integrated (low BOM, easy design-in)
- No alignment required in production
- Fast settling, programmable, high-resolution PLL
- Fast frequency hopping capability
- Stable and accurate FSK modulation with programmable deviation
- Programmable PLL loop bandwidth
- Direct loop antenna drive
- Automatic antenna tuning circuit
- Programmable output power level
- SPI bus for applications with microcontroller
- Clock output for microcontroller
- Integrated programmable crystal load capacitor
- Multiple event handling options for wake-up activation
- Wake-up timer
- Low battery detection
- 2.2V to 5.4V supply voltage
- Low power consumption
- Low standby current (0.3 μA)
- Transmit bit synchronization

TYPICAL APPLICATIONS

- Remote control
- Home security and alarm
- Wireless keyboard/mouse and other PC peripherals
- Toy control
- Remote keyless entry
- Tire pressure monitoring
- Telemetry
- Personal/patient data logging
- Remote automatic meter reading

DETAILED FEATURE-LEVEL DESCRIPTION

The RFM02 FSK transmitter is designed to cover the unlicensed frequency bands at 433, 868, and 915 MHz. The device facilitates compliance with FCC and ETSI requirements.

PLL

The programmable PLL synthesizer determines the operating frequency, while preserving accuracy based on the on-chip crystal-controlled reference oscillator. The PLL's high resolution allows the usage of multiple channels in any of the bands. The FSK deviation is selectable (from 30 to 210 kHz with 30 kHz increments) to accommodate various bandwidth, data rate and crystal tolerance requirements, and it is also highly accurate due to the direct closed-loop modulation of the PLL. The transmitted digital data can be sent asynchronously through the FSK pin or over the control interface using the appropriate command.

RF Power Amplifier (PA)

The power amplifier has an open-collector differential output and can directly drive a loop antenna with a programmable output power level. An automatic antenna tuning circuit is built in to avoid costly trimming procedures and the so-called "hand effect."

Crystal Oscillator

The chip has a single-pin crystal oscillator circuit, which provides a 10 MHz reference signal for the PLL. To reduce external parts and simplify design, the crystal load capacitor is internal and programmable. Guidelines for selecting the appropriate crystal can be found later in this datasheet.

The transmitters can supply the clock signal for the microcontroller, so accurate timing is possible without the need for a second crystal. When the chip receives a Sleep Command from the microcontroller and turns itself off, it provides several further clock pulses (“clock tail”) for the microcontroller to be able to go to idle or sleep mode. The length of the clock tail is programmable.

Low Battery Voltage Detector

The low battery voltage detector circuit monitors the supply voltage and generates an interrupt if it falls below a programmable threshold level.

Wake-Up Timer

The wake-up timer has very low current consumption (1.5 uA typical) and can be programmed from 1 ms to several days with an accuracy of ±5%.

It calibrates itself to the crystal oscillator at every startup, and then every 30 seconds. When the oscillator is switched off, the calibration circuit switches on the crystal oscillator only long enough for a quick calibration (a few milliseconds) to facilitate accurate wake-up timing.

Event Handling

In order to minimize current consumption, the device supports sleep mode. Active mode can be initiated by several wake-up events: timeout of wake-up timer, detection of low supply voltage or through the serial interface.

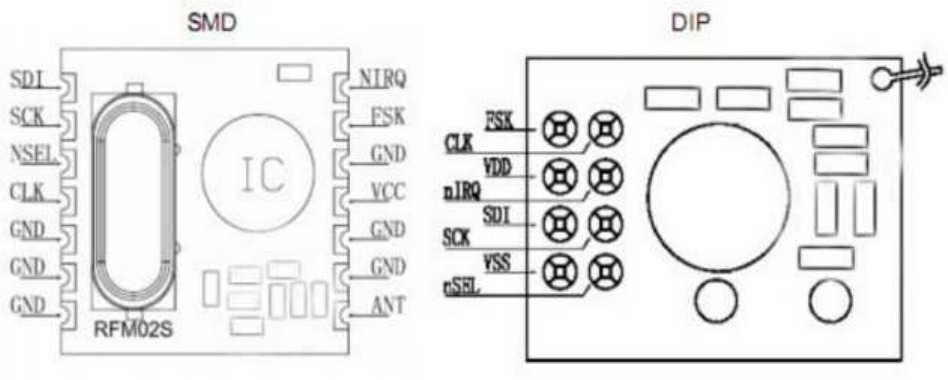
If any wake-up event occurs, the wake-up logic generates an interrupt, which can be used to wake up the microcontroller, effectively reducing the period the microcontroller has to be active. The cause of the interrupt can be read out from the transmitters by the microcontroller through the nIRQ pin.

Interface

An SPI compatible serial interface lets the user select the operating frequency band and center frequency of the synthesizer, polarity and deviation of FSK modulation, and output power level. Division ratio for the microcontroller clock, wake-up timer period, and low battery detector threshold are also programmable. Any of these auxiliary functions can be disabled when not needed. All parameters are set to default after power-on; the programmed values are retained during sleep mode.

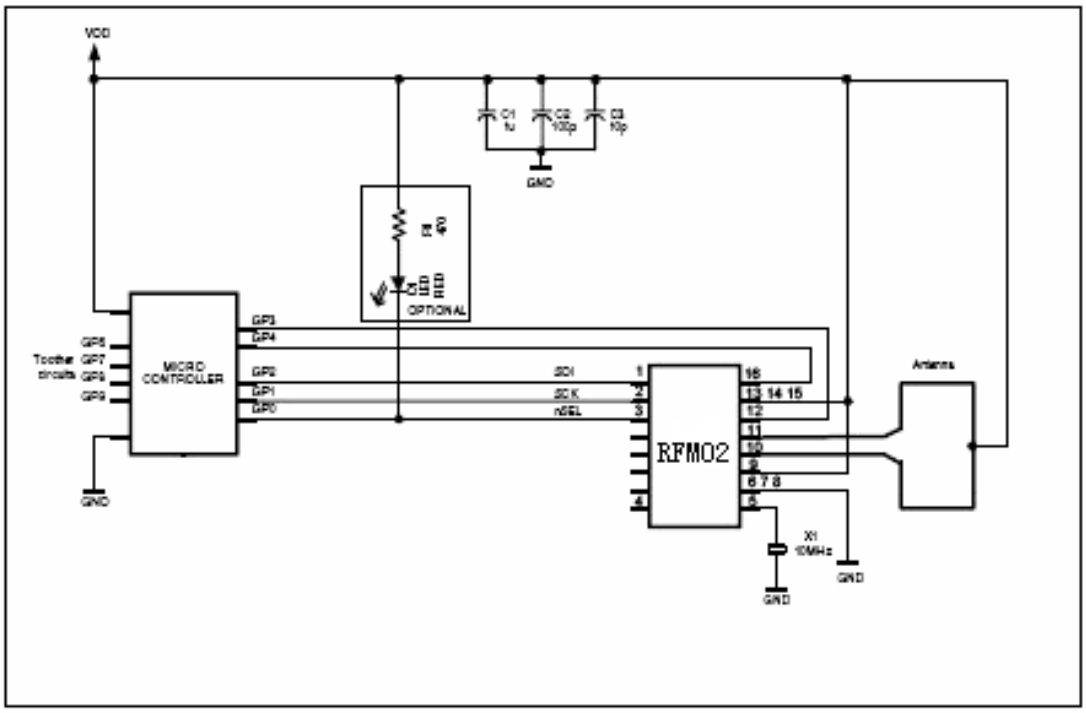
PACKAGE PIN DEFINITIONS

Pin type key: D=digital, A=analog, S=supply, I=input, O=output, IO=input/output



Definition	TYPE	function
FSK	DI	FSK data input
CLK	DO	clock out for MCU (1 MHz-10 MHz)
VDD	S	Positive power supply
nIRQ	DO	Interrupts request output（active low）
SDI	DI	SPI data input
SCK	DI	SPI clock input
VSS	S	negative power supply, GND
nSEL	DI	Chip select (active low)

Typical application



GENERAL DEVICE SPECIFICATION

All voltages are referenced to V_{ss}, the potential on the ground reference pin VSS.

Absolute Maximum Ratings (non-operating)

Symbol	Parameter	Min	Max	Units
V_{dd}	Positive supply voltage	-0.5	6.0	V
V_{in}	Voltage on any pin except open collector outputs	-0.5	V_{dd}+0.5	V
V_{oc}	Voltage on open collector outputs	-0.5	6.0	V
I_{in}	Input current into any pin except VDD and VSS	-25	25	mA
ESD	Electrostatic discharge with human body model		1000	V
T_{st}	Storage temperature	-55	125	℃

Recommended Operating Range

Symbol	Parameter	Min	Max	Units
V_{dd}	Positive supply voltage	2.2	5.4	V
V_{oc}	Voltage on open collector outputs (Max 6.0 V)	V_{dd} - 1	V_{dd} + 1	V
T_{op}	Ambient operating temperature	-40	85	℃

ELECTRICAL SPECIFICATION

(Min/max values are valid over the whole recommended operating range, typ conditions:

T_{op} =27℃;V_{dd} =V_{oc}=2.7V)

DC Characteristics

Symbol	Parameter		Conditions/Notes	Min	Typ	Max	Units
$I_{dd\_TX\_0}$	Supply current (TX mode, Pout =0dBm)	433 MHz band 868 MHz band 915 MHz band	Active state with 0dBm output power		12 14 15		mA
$I_{dd\_TX\_PMAX}$	Supply current (TX mode, Pout =P_{max})	433 MHz band 868 MHz band 915 MHz band	Active state with maximum output power		21 23 24		mA
I_{pd}	Standby current in sleep mode (Note 1)		All blocks disabled		0.3		µA
I_{wt}	Wake-up timer current consumption				1.5		µA
I_{lb}	Low battery detector current consumption				0.5		µA
I_x	Idle current		Only crystal oscillator is on		1.5		mA

V_{lba}	Low battery detection accuracy			+/-3		%
V_{lb}	Low battery detector threshold	Programmable in 0.1 V steps	2.2		5.3	V
V_{il}	Digital input low level				$0.3*V_{dd}$	V
V_{ih}	Digital input high level		$0.7*V_{dd}$			V
I_{il}	Digital input current	V_{il} = 0 V	-1		1	µA
I_{ih}	Digital input current	$V_{ih} = V_{dd}$, V_{dd} = 5.4 V	-1		1	µA
V_{ol}	Digital output low level	I_{ol} = 2 mA			0.4	V
V_{oh}	Digital output high level	I_{oh} = -2 mA	V_{dd}-0.4			V

AC Characteristic

Symbol	Parameter	Conditions/Notes	Min	Typ	Max	Units
f_{ref}	PLL reference frequency	Crystal operation mode is parallel (Note 2)	9	10	11	MHz
f_o		433MHz band, 2.5kHz resolution 868MHz band, 5.0kHz resolution 915MHz band, 7.5kHz resolution	430.24 860.48 900.72		439.75 879.51 929.27	MHz
t_{lock}	PLL lock time	Frequency error < 10 kHz after 10 MHz step, POR default PLL setting(Note 7)		20		µs
t_{sp}	PLL startup time	After turning on from idle mode, with crystal oscillator already stable, POR default PLL setting (Note 7)			250	µs
I_{OUT}	Open collector output current (Note 3)	At all bands	0.5		6	mA
P_{maxL}	Available output power (433MHz band)	With opt. antenna impedance (Note 4)		8		dBm
P_{maxH}	Available output power (868 and 915 MHz band)	With opt. antenna impedance (Note 4)		6		dBm
P_{out}	Typical output power	Selectable in 3 dB steps (Note 3)	P_{max}-21		P_{max}	dBm
P_{sp}	Spurious emission	At max power with loop antenna (Note 5)			-50	dBc

C_o	Output capacitance (set by the automatic antenna tuning circuit)	At low bands At high bands	1.5 1.6	2.3 2.2	2.8 3.1	pF
Q_o	Quality factor of the output capacitance		16	18	22	pF
L_{out}	Output phase noise	100 kHz from carrier 1 MHz from carrier (Note 7)		-85 -105		dBc/Hz
BR_{FSK}	FSK bit rate	(Note 7)			115.2	kbps
df_{fsk}	FSK frequency deviation	Programmable in 30 kHz steps	30		210	kHz
C_{xl}	Crystal load capacitance See Crystal Selection Guidelines	Programmable in 0.5 pF steps, tolerance +/-10%	8.5		16	pF
t_{POR}	Internal POR timeout (Note 6)	After V_{dd} has reached 90% of final value			50	ms
t_{sx}	Crystal oscillator startup time	Crystal ESR < 100 Ohms		1.5	5	ms
t_{PBt}	Wake-up timer clock period	Calibrated every 30 seconds	0.95		1.05	ms
$t_{wake-up}$	Programmable wake-up time		1		$5 *10^{11}$	ms
$C_{in, D}$	Digital input capacitance				2	pF
$t_{r, f}$	Digital output rise/fall time	15 pF pure capacitive load			10	ns

Note 1: Using a CR2032 battery (225 mAh capacity), the expected battery life is greater than 2 years using a 60-second wake-up period for sending 50 byte packets in length at 19.2 kbps with +6 dBm output power in the 915 MHz band.

Note 2: Using anything but a 10 MHz crystal is allowed but not recommended because all crystal-referred timing and frequency parameters will change accordingly.

Note 3: Adjustable in 8 steps.

Note 4: Optimal antenna admittance/impedance for the RFM02:

	Yantenna [S]	Zantenna [Ohm]	Lantenna [nH]
434 MHz	1.3E-3 - j6.3E-3	31 + j152	58.00
868 MHz	1.35E-3 - j1.2E-2	9 + j82	15.20
915 MHz	1.45E-3 - j1.3E-2	8.7 + j77	13.60

Note 5: With selective resonant antennas .

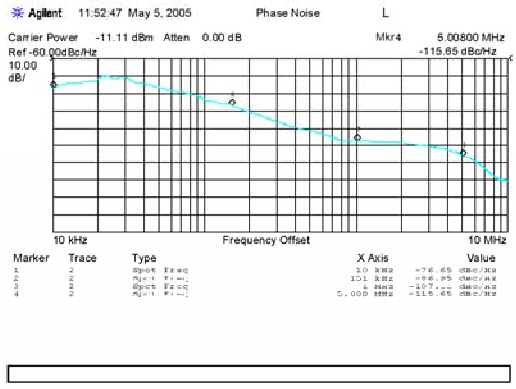
Note 6: During this period, no commands are accepted by the chip.

Note 7: The maximum FSK bitrate and the Output phase noise are dependent on the actual setting of the PLL Setting Command.

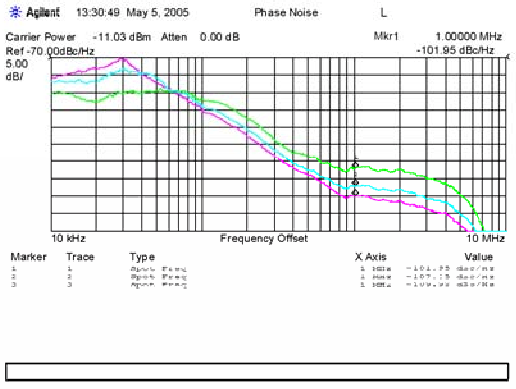
TYPICAL PERFORMANCE DATA (RFM02)

Phase noise measurements in the 868 MHz ISM band

50% Charge pump current setting
(Ref. level: -60 dBc/Hz, 10 dB/div)



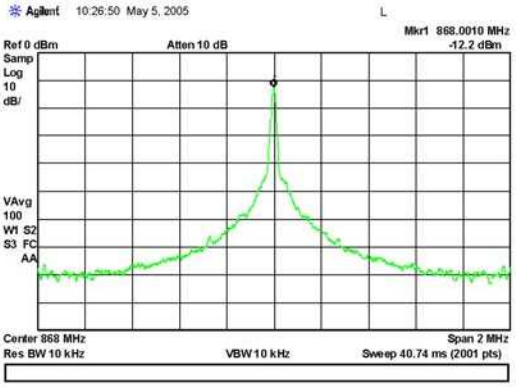
100, 50, 33% Charge pump current settings
(Ref. level: -70 dBc/Hz, 5 dB/div)



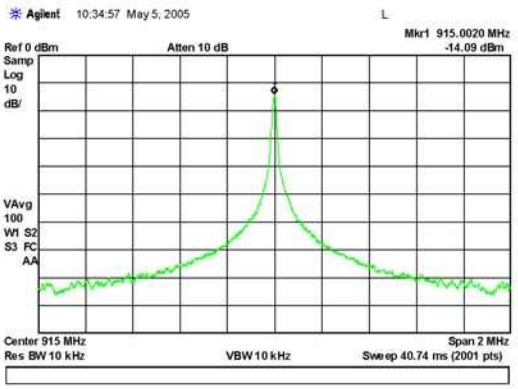
Unmodulated RF Spectrum

The output spectrum is measured at different frequencies. The output is loaded with 50 Ohms through a matching network.

At 868 MHz

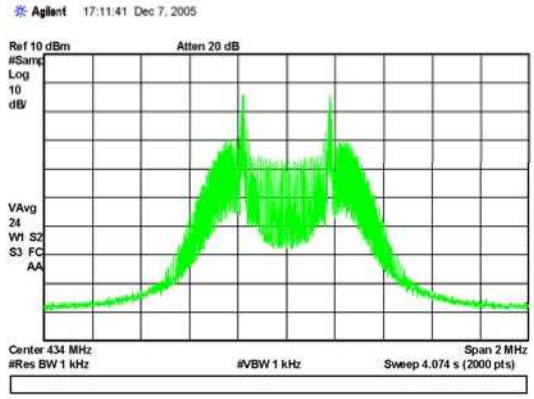


At 915 MHz

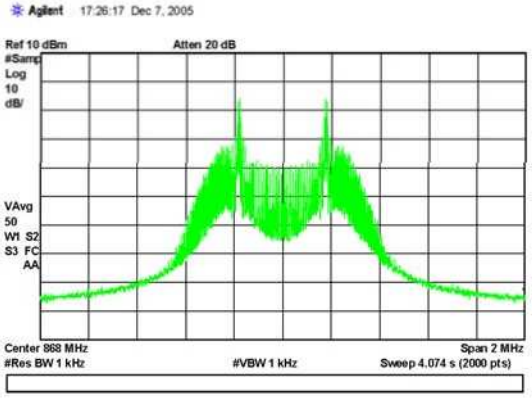


Modulated RF Spectrum

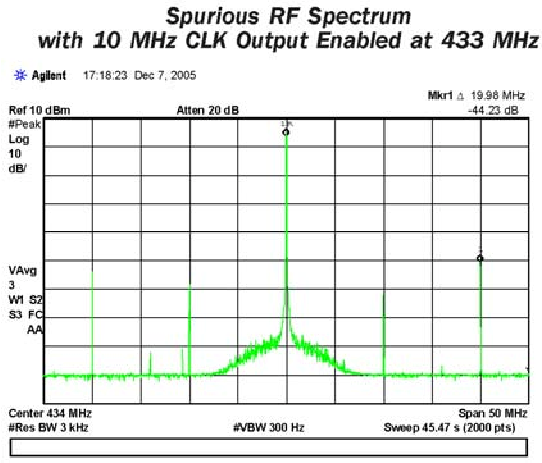
At 433 MHz with
180 kHz Deviation at 9.6 kbps

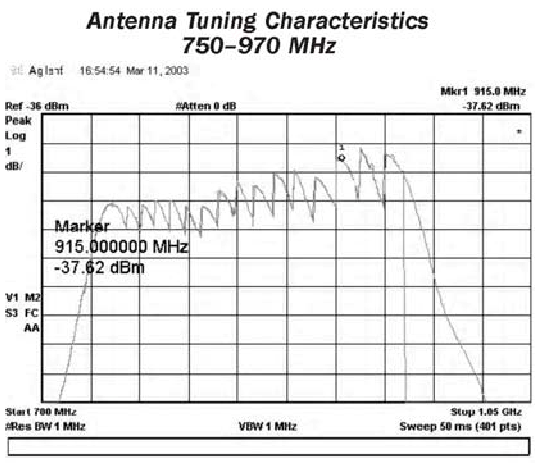


At 868 MHz with
180 kHz Deviation at 9.6 kbps



Other Important Characteristics





The antenna tuning characteristics was recorded in “max-hold” state of the spectrum analyzer. During the measurement, the transmitters were forced to change frequencies by forcing an external reference signal to the XTL pin. While the carrier was changing the antenna tuning circuit switched trough all the available states of the tuning circuit. The graph clearly demonstrates that while the complete output circuit had about a 40 MHz bandwidth, the tuning allows operating in a 220 MHz band. In other words the tuning circuit can compensate for 25% variation in the resonant frequency due to any process or manufacturing spread.

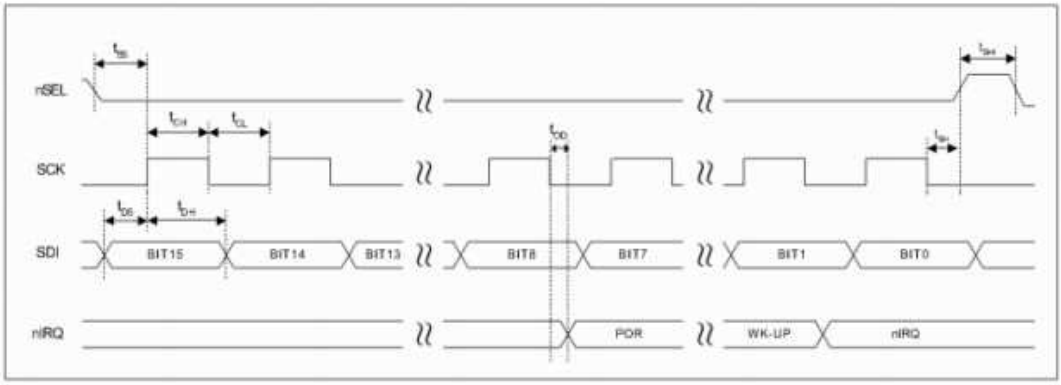
CONTROL INTERFACE

Commands to the transmitters are sent serially. Data bits on pin SDI are shifted into the device upon the rising edge of the clock on pin SCK whenever the chip select pin nSEL is low. When the nSEL signal is high, it initializes the serial interface. The number of bits sent is an integer multiple of 8. All commands consist of a command code, followed by a varying number of parameter or data bits. All data are sent MSB first (e.g. bit 15 for a 16-bit command). Bits having no influence (don’t care) are indicated with X. The Power On Reset (POR) circuit sets default values in all control and command registers.

Timing Specification

Symbol	Parameter	Minimum Value [ns]
t_{CH}	Clock high time	25
t_{CL}	Clock low time	25
t_{SS}	Select setup time (nSEL falling edge to SCK rising edge)	10
t_{SH}	Select hold time (SCK falling edge to nSEL rising edge)	10
t_{SHI}	Select high time	25
t_{DS}	Data setup time (SDI transition to SCK rising edge)	5
t_{DH}	Data hold time (SCK rising edge to SDI transition)	5
t_{OD}	Data delay time	10

Timing Diagram



Control Commands

	Control Command	Related Parameters/Functions
1	Configuration Setting Command	Frequency band, microcontroller clock output, crystal load capacitance, frequency deviation
2	Power Management Command	Crystal oscillator, synthesizer, power amplifier, low battery detector, wake-up timer, clock output buffer
3	Frequency Setting Command	Carrier frequency
4	Data Rate Command	Bit rate
5	Power Setting Command	Nominal output power, OOK mode
6	Low Battery Detector Command	Low battery threshold limit
7	Sleep Command	Length of the clock tail after power down
8	Wake-Up Timer Command	Wake-up time period
9	Data Transmit Command	Data transmission
10	Status Register Command	Transmitter status read
11	PLL Setting Command	PLL bandwidth can be modified by this command

Note: In the following tables the POR column shows the default values of the command registers after power-on.

1. Configuration Setting Command

bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0	POR
	1	0	0	b1	b0	d2	d1	d0	x3	x2	x1	x0	ms	m2	m1	m0	8080h

b1	b0	Frequency Band [MHz]
0	1	433
1	0	868
1	1	915

x3	x2	x1	x0	Crystal Load Capacitance [pF]
0	0	0	0	8.5
0	0	0	1	9.0
0	0	1	0	9.5
		1	1	16.0
……				……
1	1	1	0	15.5

d2	d1	d0	Clock Output Frequency [MHz]
0	0	0	1
0	0	1	1.25
0	1	0	1.66
0	1	1	2
1	0	0	2.5
1	0	1	3.33
1	1	0	5
1	1	1	10

The resulting output frequency can be calculated as:

$f_{out} = f0 – (-1)^{SIGN} * (M + 1) * (30 kHz)$

where:

f0 is the channel center frequency (see the next command)

M is the three bit binary number <m2 : m0>

SIGN = (ms) XOR (FSK input)

Note:

• Use M in a range from 0 to 6.

2. Power Management Command

bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0	POR
	1	1	0	0	0	0	0	0	a1	a0	ex	es	ea	eb	et	dc	C000h

Bits 5-0, enable the corresponding block of the transmitters, i.e. the crystal oscillator is enabled by the ex bit, the synthesizer by es, the power amplifier by ea and the low battery detector by eb, while the wake-up timer by et. The bit dc disables the clock output buffer.

When receiving the Data Transmit Command, the chip supports automatic on/off control over the crystal oscillator, the PLL and the PA.

If bit a1 is set, the crystal oscillator and the synthesizer are controlled automatically. Data Transmit Command starts up the crystal oscillator and as soon as a stable reference frequency is available the synthesizer starts. After a subsequent delay to allow locking of the PLL, if a0 is set the power amplifier is turned on as well.

Note:

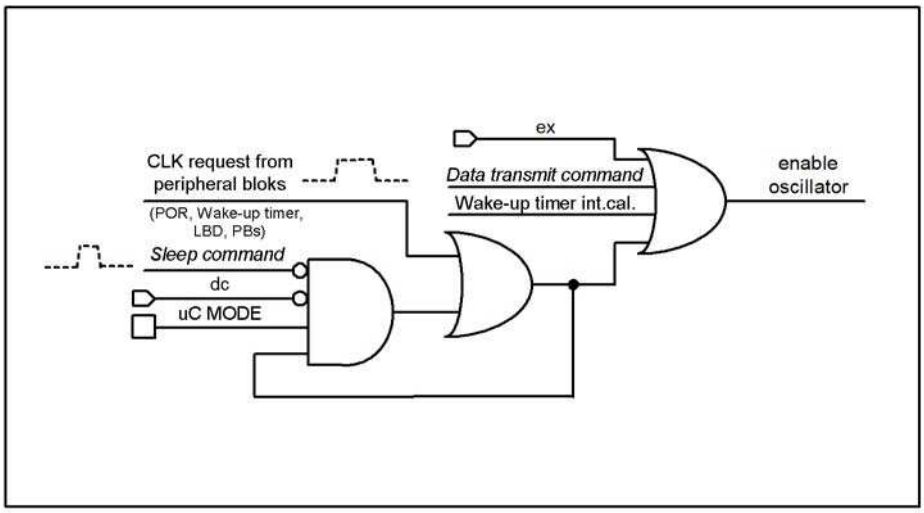
To enable the automatic internal control of the crystal oscillator, the synthesizer and the power amplifier, the corresponding bits (ex, es, ea) must be zero in the Power Management Command.

The ex bit should be set in the Power Management Command for the correct control of es and ea. The oscillator can be switched off by clearing the ex bit after the transmission.

The Sleep Command can be used to indicate the end of the data transmission process.

For processing the events caused by the peripheral blocks (POR, LBD or wake-up timer) the chip requires operation of the crystal oscillator. This operation is fully controlled internally, independently from the status of the ex bit, but if the dc bit is zero, the oscillator remains active until Sleep Command is issued. (This command can be considered as an event controller reset.)

Oscillator control logic



3. Frequency Setting Command

bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0	POR
	1	0	1	0	f11	f10	f9	f8	f7	f6	f5	f4	f3	f2	f1	f0	A7D0h

The 12-bit parameter of the Frequency Setting Command <f11 : f0> has the value F. The value F should be in the range of 96 and 3903. When F is out of range, the previous value is kept. The synthesizer center frequency f_0 can be calculated as:

f_0 = 10 MHz * C1 * (C2 + F/4000)

The constants C1 and C2 are determined by the selected band as:

Band [MHz]	**C1**	**C2**
433	1	43
868	2	43
915	3	30

Note:

• For correct operation of the frequency synthesizer, the frequency and band of operation need to be programmed before the synthesizer is started. Directly after activation of the synthesizer, the RF VCO is calibrated to ensure proper operation in the programmed frequency band.

4. Data Rate Command

bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0	POR
	1	1	0	0	1	0	0	0	r7	r6	r5	r4	r3	r2	r1	r0	C800h

The transmitted bit rate is determined by the 8-bit value R (bits *<r7 : r0>)* as:

BR = 10 MHz / 29 / (R+1)

Apart from setting custom values, the standard bit rates from 2.4 to 115.2 kbps can be approximated with minimal error.

Note:

• PLL bandwidth should be set according the data rate. Please see the *PLL Setting Command*.

5. Power Setting Command

bit	7	6	5	4	3	2	1	0	POR
	1	0	1	1	0	p2	p1	p0	B0h

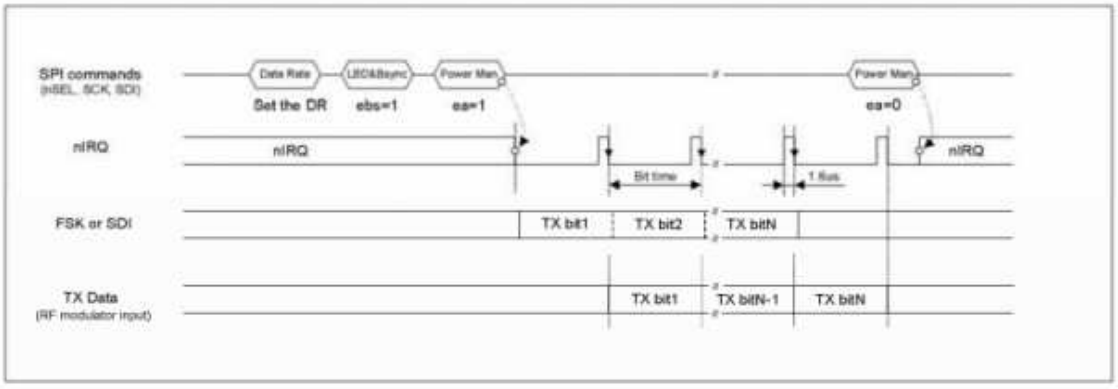
2	p1	p0	Output Power [dB]
0	0	0	0
0	0	1	-3
0	1	0	-6
0	1	1	-9
1	0	0	-12
1	0	1	-15
1	1	0	-18
1	1	1	-21

The output power is given in the table as relative to the maximum available power, which depends on the actual antenna impedance.

6. Low Battery Detector and TX Bit Synchronization Command

bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0	POR
	1	1	0	0	0	0	1	0	dwc	0	ebs	t4	t3	t2	t1	t0	C200h

Bit 7 <dwc> Disables the Wake-up timer periodical (every 30 second) calibration if this bit is set.
Bit 5 <ebs> Enables the TX bit synchronization circuit. The data rate must be set by the Data Rate Command.5



The 5-bit value T of <t4 : t0> determines the threshold voltage V_{lb} of the detector:

$$V_{lb} = 2.2\ V + T * 0.1\ V$$

7. Sleep Command

bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0	POR
	1	1	0	0	0	1	0	0	s7	s6	s5	s4	s3	s2	s1	s0	C400h

The effect of this command depends on the Power Management Command. It immediately disables the power amplifier (if a0=1 and ea=0) and the synthesizer (if a1=1 and es=0). Stops the crystal oscillator

after S periods of the microcontroller clock (if a1=1 and ex=0) to enable the microcontroller to execute all necessary commands before entering sleep mode itself. The 8-bit value S is determined by bits <s7:s0>.

8. Wake-Up Timer Command

bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0	POR
	1	1	1	r4	r3	r2	r1	r0	m7	m6	m5	m4	m3	m2	m1	m0	E000h

The wake-up time period can be calculated as:

$$T_{wake\text{-}up} = M * 2^R \text{ [ms]},$$

where M is defined by the <m7 : m0> digital value and R is defined by the <r4 : r0> digital value.

Note:

- For continual operation the et bit should be cleared and set at the end of every cycle.

9. Data Transmit Command

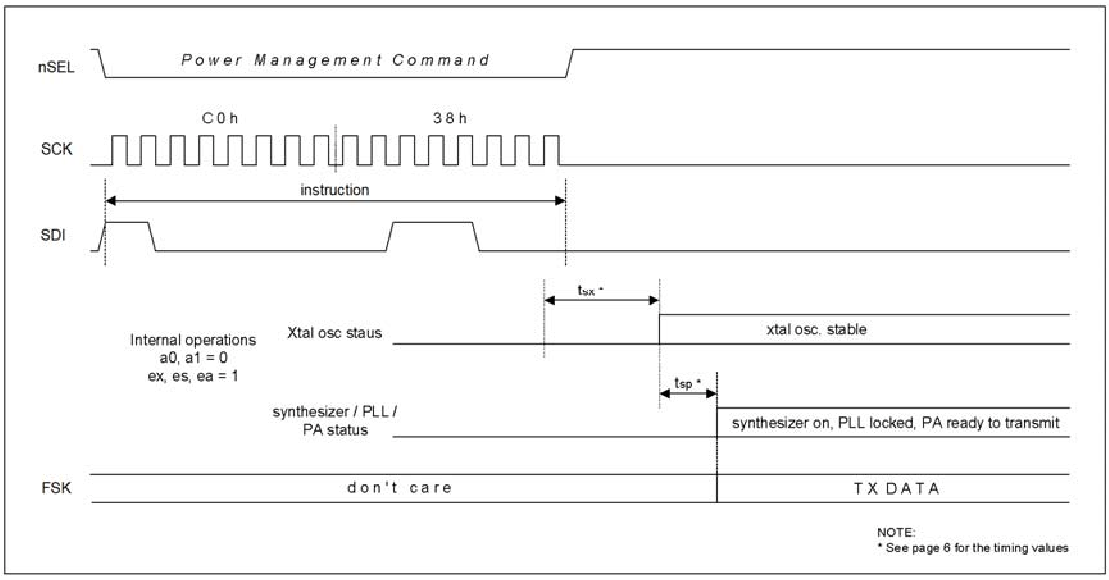
bit	7	6	5	4	3	2	1	0
	1	1	0	0	0	1	1	0

This Command Indicates that the following bitstream coming in via the serial interface is to be transmitted.

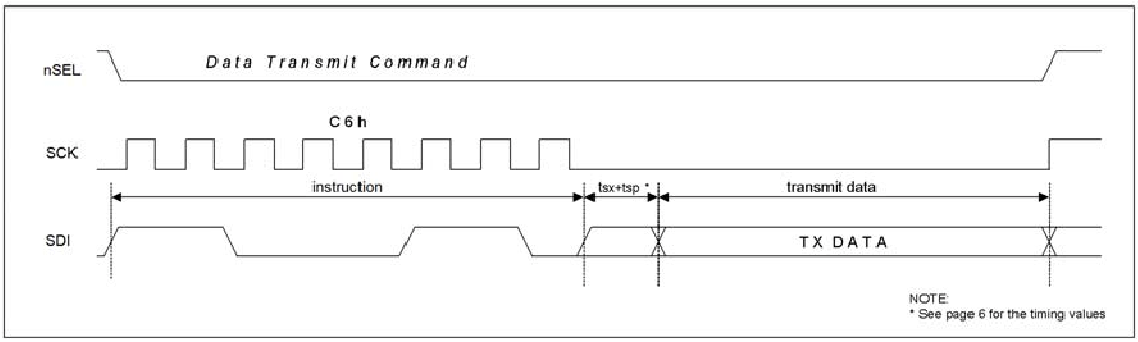
Note

- This command is not needed if the transmitters' power management bits (*ex, es and ea*) are fully controlled by the microcontroller and TX data comes through the FSK pin.
- If the crystal oscillator was formerly switched off (*ex*=0), the internal oscillator needs t_{sx} time, to switch on. The actual value depends on the type of quartz crystal used.
- If the synthesizer was formerly switched off (*es*=0), the internal PLL needs t_{sp} startup time. Valid data can be transmitted only when the internal locking process is finished.

Data Transmit Sequence Through the FSK Pin



Data Transmit Sequence Through the SDI Pin



Note:

Do not send CLK pulses with the TX data bits, otherwise they will be interpreted as commands.

This mode is not SPI compatible.

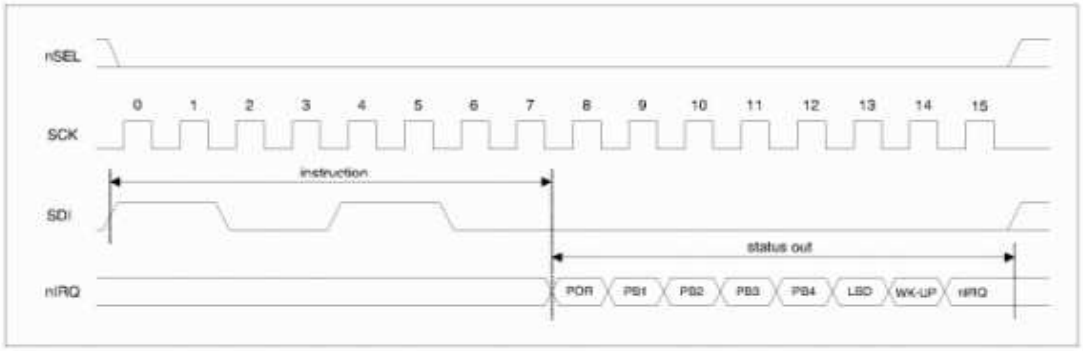
If the crystal oscillator and the PLL are running, the t_{sx}+t_{sp} delay is not needed.

10 . Status Register Read Command

bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0	POR
	1	1	0	0	1	1	0	0	0	0	0	0	0	0	0	0	--

With this command, it is possible to read the chip's status register through the nIRQ pin. This command clears the last serviced interrupt and processing the next pending one will start (if there is any).

Status Register Read Sequence



11. PLL Setting Command

PLL bandwidth can be selected by this command

PLL command	Max data rate [kbps]	Phase noise at 1MHz offset [dbc/Hz]	Comments
D240h	19.2	-112	25%current
D2C0h	38.4	-110	33%current
D200h	68.9	-107	50%current
D280h	115.2	-102	100%current

RX-TX ALIGNMENT PROCEDURES

RX-TX frequency offset can be caused only by the differences in the actual reference frequency. To minimize these errors it is suggested to use the same crystal type and the same PCB layout for the crystal placement on the RX and TX PCBs.

To verify the possible RX-TX offset it is suggested to measure the CLK output of both chips with a high level of accuracy. Do not measure the output at the XTL pin since the measurement process itself will change the reference frequency. Since the carrier frequencies are derived from the reference frequency, having identical reference frequencies and nominal frequency settings at the TX and RX side there should be no offset if the CLK signals have identical frequencies.

It is possible to monitor the actual RX-TX offset using the AFC status report included in the status byte of the receiver. By reading out the status byte from the receiver the actual measured offset frequency will be reported. In order to get accurate values the AFC has to be disabled during the read by clearing the "en" bit in the AFC Control Command (bit 0).

CRYSTAL SELECTION GUIDELINES

The crystal oscillator of the RFM02 requires a 10 MHz parallel mode crystal. The circuit contains an integrated load capacitor in order to minimize the external component count. The internal load capacitance value is programmable from 8.5 pF to 16 pF in 0.5 pF steps. With appropriate PCB layout, the total load capacitance value can be 10 pF to 20 pF so a variety of crystal types can be used.

When the total load capacitance is not more than 20 pF and a worst case 7 pF shunt capacitance (C0) value is expected for the crystal, the oscillator is able to start up with any crystal having less than 100 ohms ESR (equivalent series loss resistance). However, lower C0 and ESR values guarantee faster oscillator startup. It is recommended to keep the PCB parasitic capacitances on the XTL pin as low as possible.

The crystal frequency is used as the reference of the PLL, which generates the RF carrier frequency (fc). Therefore fc is directly proportional to the crystal frequency. The accuracy requirements for production tolerance, temperature drift and aging can thus be determined from the maximum allowable carrier frequency error.

Maximum XTAL Tolerances Including Temperature and Aging [ppm]

Bit Rate: 2.4kbps	Transmitter Deviation [+/- kHz]						
	30	60	90	120	150	180	210
315 MHz	30	75	100	100	100	100	100
433 MHz	20	50	75	100	100	100	100
868 MHz	10	25	40	60	75	100	100
915 MHz	10	25	40	50	75	75	100

Bit Rate: 9.6kbps	Transmitter Deviation [+/- kHz]						
	30	60	90	120	150	180	210
315 MHz	25	70	100	100	100	100	100
433 MHz	15	50	75	100	100	100	100
868 MHz	8	25	40	60	75	75	100
915 MHz	8	25	40	50	70	75	100

Bit Rate: 38.3kbps	Transmitter Deviation [+/- kHz]						
	30	60	90	120	150	180	210
315 MHz	don't use	30	75	100	100	100	100
433 MHz	don't use	20	50	75	100	100	100
868 MHz	don't use	10	30	40	60	75	100
915 MHz	don't use	10	25	40	60	75	75

Whenever a low frequency error is essential for the application, it is possible to “pull” the crystal to the accurate frequency by changing the load capacitor value. The widest pulling range can be achieved if the nominal required load capacitance of the crystal is in the “midrange”, for example 16 pF. The “pull-ability” of the crystal is defined by its motional capacitance and C_0

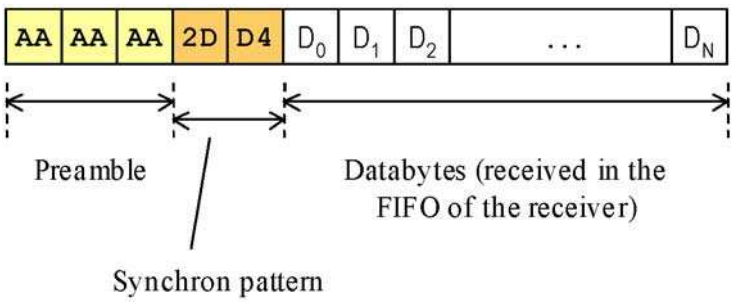
Note:

• There may be other requirements for the TX carrier accuracy with regards to the requirements as defined by standards and/or channel separations.

EXAMPLE APPLICATIONS: DATA PACKET TRANSMISSION

Data packet structure

An example data packet structure using the RFM02X - RF01 pair for data transmission. This packet structure is an example of how to use the high efficiency FIFO mode at the receiver side:



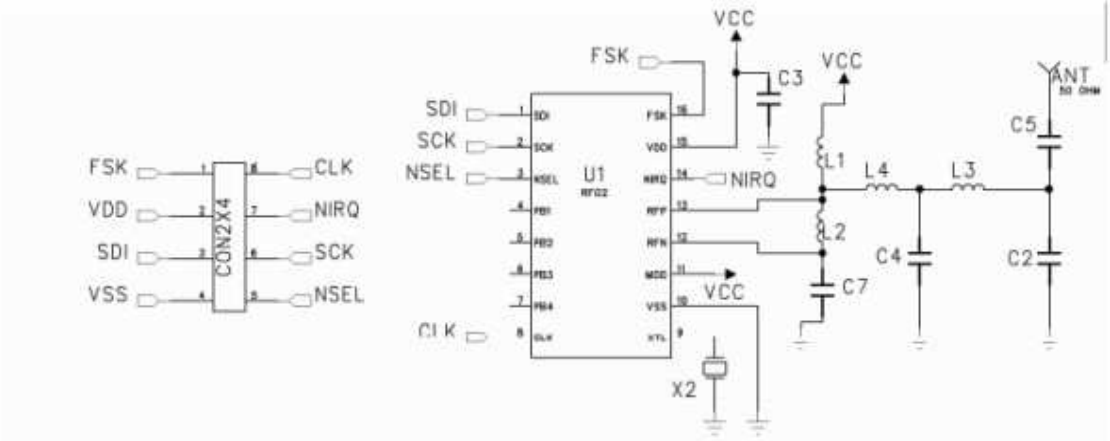
The first 3 bytes compose a 24 bit length ‘01’ pattern to let enough time for the clock recovery of the receiver to lock. The next two bytes compose a 16 bit synchron pattern which is essential for the receiver’s FIFO to find the byte synchron in the received bit stream. The synchron patters is followed by the payload. The first byte transmitted after the synchron pattern (D0 in the picture above) will be the first received byte in the FIFO.

Important: The bytes of the data stream should follow each other continuously, otherwise the clock recovery circuit of the receiver side will be unable to track.

Further details of packet structures can be found in the RF ISM-UGSB1 software development kit manual

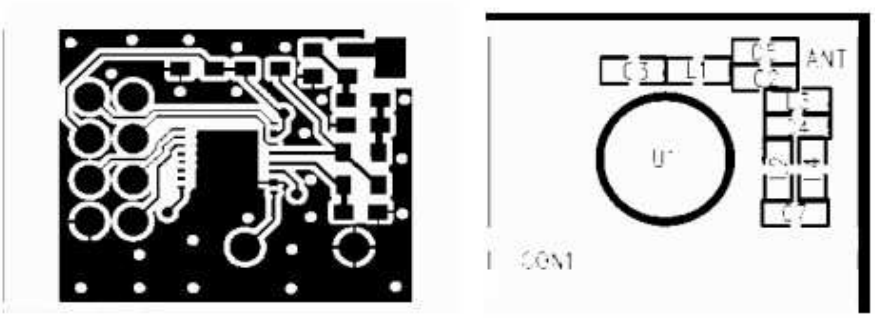
REFERENCE DESIGNS

Schematic

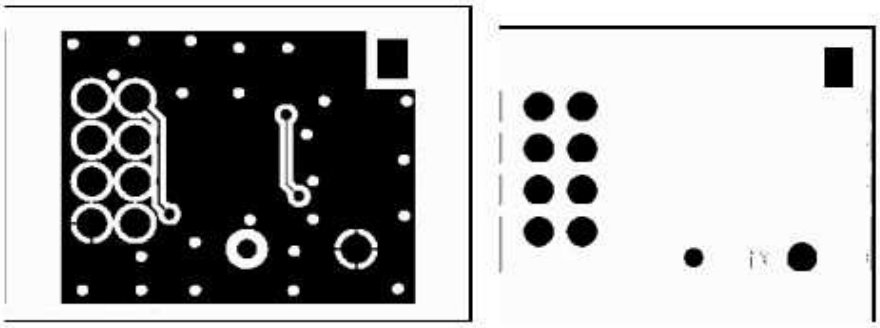


	C3	L1	L2	C7	L4	C4	L3	C2	C5
434	10nF	220nH	27nH	4.7PF	22nH	10PF	27nH	12PF	5.6PF
869	10nF	47nH	10nH	3.3PF	8.2nH	3.9PF	15nH	3.9PF	5.6PF
915	10nF	47nH	10nH	3.3PF	8.2nH	3.3PF	15nH	3.9PF	5.6PF

PCB layout

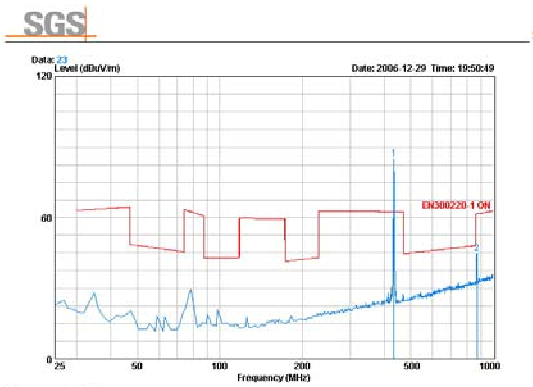


Top view



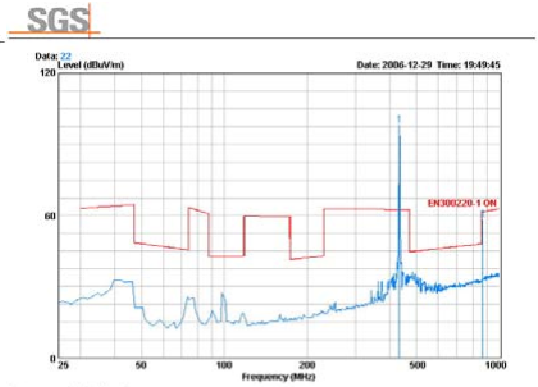
Bottom view

SGS Reports



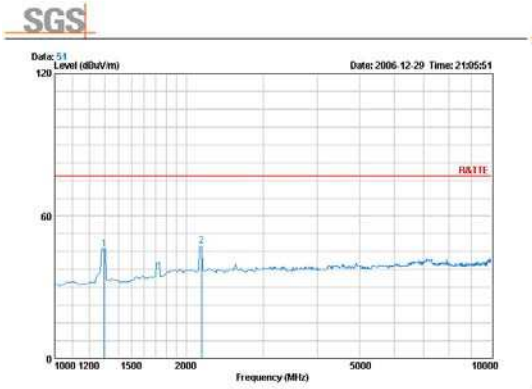
Site : 3m-chamber site
Condition : EN300220-1 ON 3m 0042673 HORIZONTAL
EUT : #A

	Freq	Cable Loss	Antenna Factor	Preamp Factor	Read Level	Level	Limit Line	Over Limit
	MHz	dB	dB/m	dB	dBuV	dBuV/m	dBuV/m	dB
1 P	432.550	2.34	16.56	27.52	93.56	84.94	62.55	22.39
2	872.275	3.50	22.93	26.57	44.93	44.80	61.61	-16.82



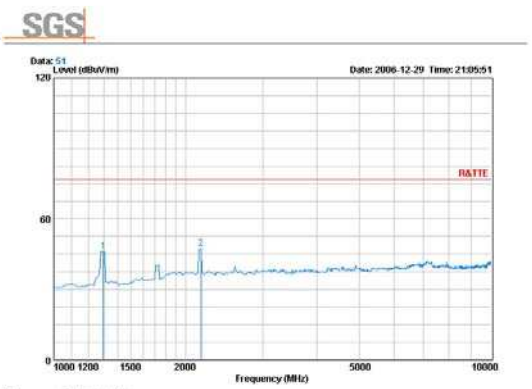
Site : 3m-chamber site
Condition : EN300220-1 ON 3m 0042673 VERTICAL
EUT : #A

	Freq	Cable Loss	Antenna Factor	Preamp Factor	Read Level	Level	Limit Line	Over Limit
	MHz	dB	dB/m	dB	dBuV	dBuV/m	dBuV/m	dB
1 P	432.550	2.34	16.56	27.52	106.57	97.95	62.55	35.41
2	868.375	3.48	22.85	26.58	58.53	58.28	61.57	-3.29



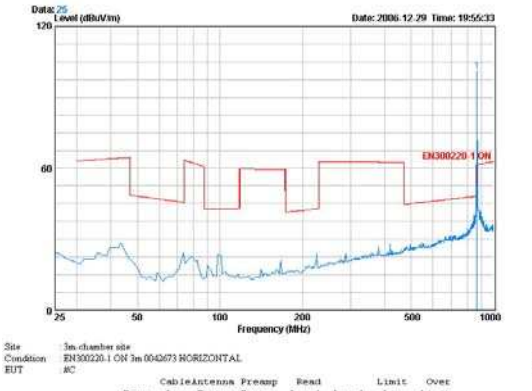
Site : 3m-chamber site
Condition : R&TTE 3m 3117 VERTICAL
EUT : #A

	Freq	Cable Loss	Antenna Factor	Preamp Factor	Read Level	Level	Limit Line	Over Limit
	MHz	dB	dB/m	dB	dBuV	dBuV/m	dBuV/m	dB
1	1297.000	1.28	27.66	44.76	61.95	46.13	77.00	-30.87
2 P	2170.000	1.84	32.11	44.70	58.10	47.35	77.00	-29.65



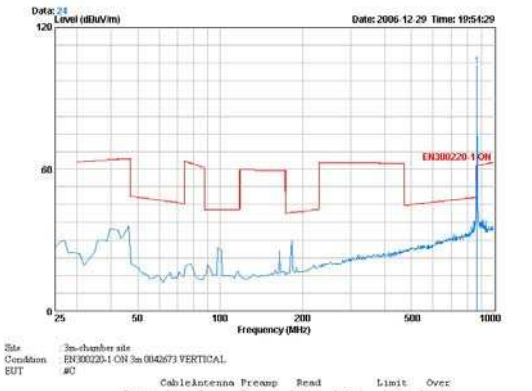
Site : 3m-chamber site
Condition : R&TTE 3m 3117 VERTICAL
EUT : #A

	Freq	Cable Loss	Antenna Factor	Preamp Factor	Read Level	Level	Limit Line	Over Limit
	MHz	dB	dB/m	dB	dBuV	dBuV/m	dBuV/m	dB
1	1297.000	1.28	27.66	44.76	61.95	46.13	77.00	-30.87
2 P	2170.000	1.84	32.11	44.70	58.10	47.35	77.00	-29.65



Site : 3m-chamber site
Condition : EN300220-1 ON 3m 0042673 HORIZONTAL
EUT : #C

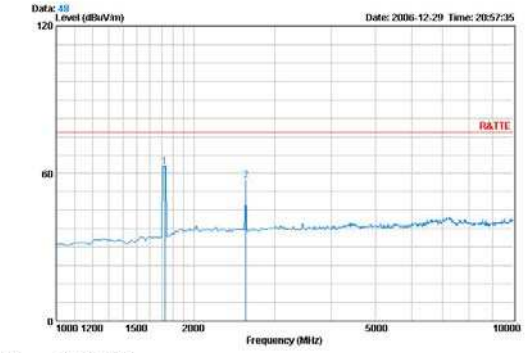
	Freq	Cable Loss	Antenna Factor	Preamp Factor	Read Level	Level	Limit Line	Over Limit
	MHz	dB	dB/m	dB	dBuV	dBuV/m	dBuV/m	dB
1 P	868.375	3.48	22.85	26.58	101.34	101.09	61.57	39.51



Site : 3m-chamber site
Condition : EN300220-1 ON 3m 0042673 VERTICAL
EUT : #C

	Freq	Cable Loss	Antenna Factor	Preamp Factor	Read Level	Level	Limit Line	Over Limit
	MHz	dB	dB/m	dB	dBuV	dBuV/m	dBuV/m	dB
1 P	868.375	3.48	22.85	26.58	103.75	103.49	61.57	41.92

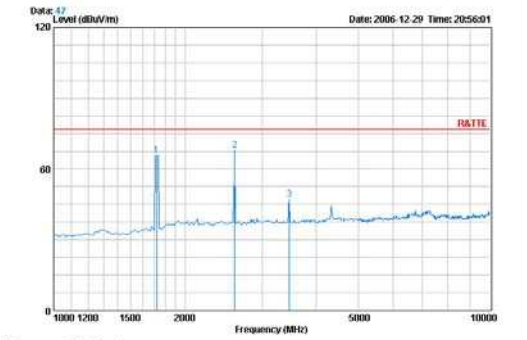
SGS



Site : 3m-chamber site
Condition : R&TTE 3m 3117 HORIZONTAL
EUT : #C

	Freq	Cable Loss	Antenna Factor	Preamp Factor	Read Level	Level	Limit Line	Over Limit
	MHz	dB	dB/m	dB	dBuV	dBuV/m	dBuV/m	dB
1 @	1729.000	1.59	29.86	44.70	76.11	62.86	77.00	-14.14
2	2602.000	2.04	32.54	44.80	67.38	57.16	77.00	-19.84

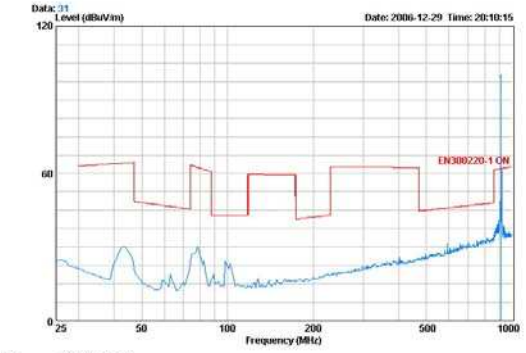
SGS



Site : 3m-chamber site
Condition : R&TTE 3m 3117 VERTICAL
EUT : #C

	Freq	Cable Loss	Antenna Factor	Preamp Factor	Read Level	Level	Limit Line	Over Limit
	MHz	dB	dB/m	dB	dBuV	dBuV/m	dBuV/m	dB
1	1720.000	1.59	29.82	44.70	78.87	65.58	77.00	-11.42
2 @	2602.000	2.04	32.54	44.80	70.13	67.91	77.00	-9.09
3	3468.000	2.35	33.21	45.01	56.47	47.02	77.00	-29.98

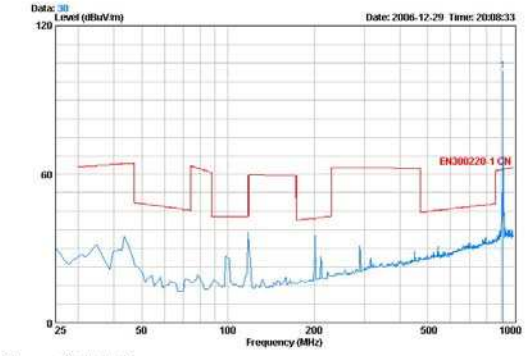
SGS



Site : 3m-chamber site
Condition : EN300220-1 ON 3m 0042673 HORIZONTAL
EUT : #E

	Freq	Cable Loss	Antenna Factor	Preamp Factor	Read Level	Level	Limit Line	Over Limit
	MHz	dB	dB/m	dB	dBuV	dBuV/m	dBuV/m	dB
1 @	914.200	3.62	23.26	26.43	95.84	96.09	62.05	34.04

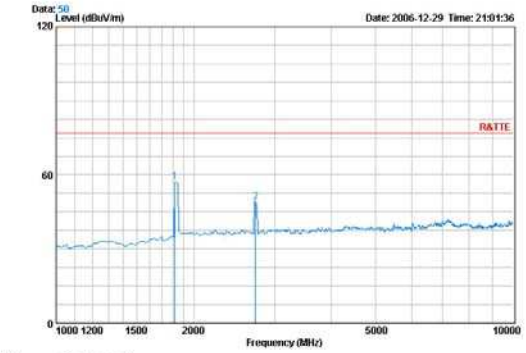
SGS



Site : 3m-chamber site
Condition : EN300220-1 ON 3m 0042673 VERTICAL
EUT : #E

	Freq	Cable Loss	Antenna Factor	Preamp Factor	Read Level	Level	Limit Line	Over Limit
	MHz	dB	dB/m	dB	dBuV	dBuV/m	dBuV/m	dB
1 @	914.200	3.62	23.26	26.43	101.18	101.63	62.05	39.57

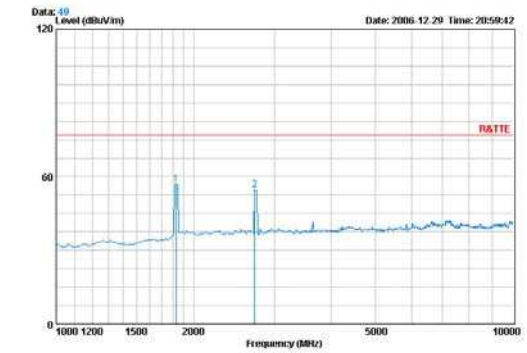
SGS



Site : 3m-chamber site
Condition : R&TTE 3m 3117 HORIZONTAL
EUT : #E

	Freq	Cable Loss	Antenna Factor	Preamp Factor	Read Level	Level	Limit Line	Over Limit
	MHz	dB	dB/m	dB	dBuV	dBuV/m	dBuV/m	dB
1 @	1819.000	1.65	30.61	44.69	69.51	57.09	77.00	-19.91
2	2728.000	2.09	32.82	44.84	58.95	49.03	77.00	-27.97

SGS



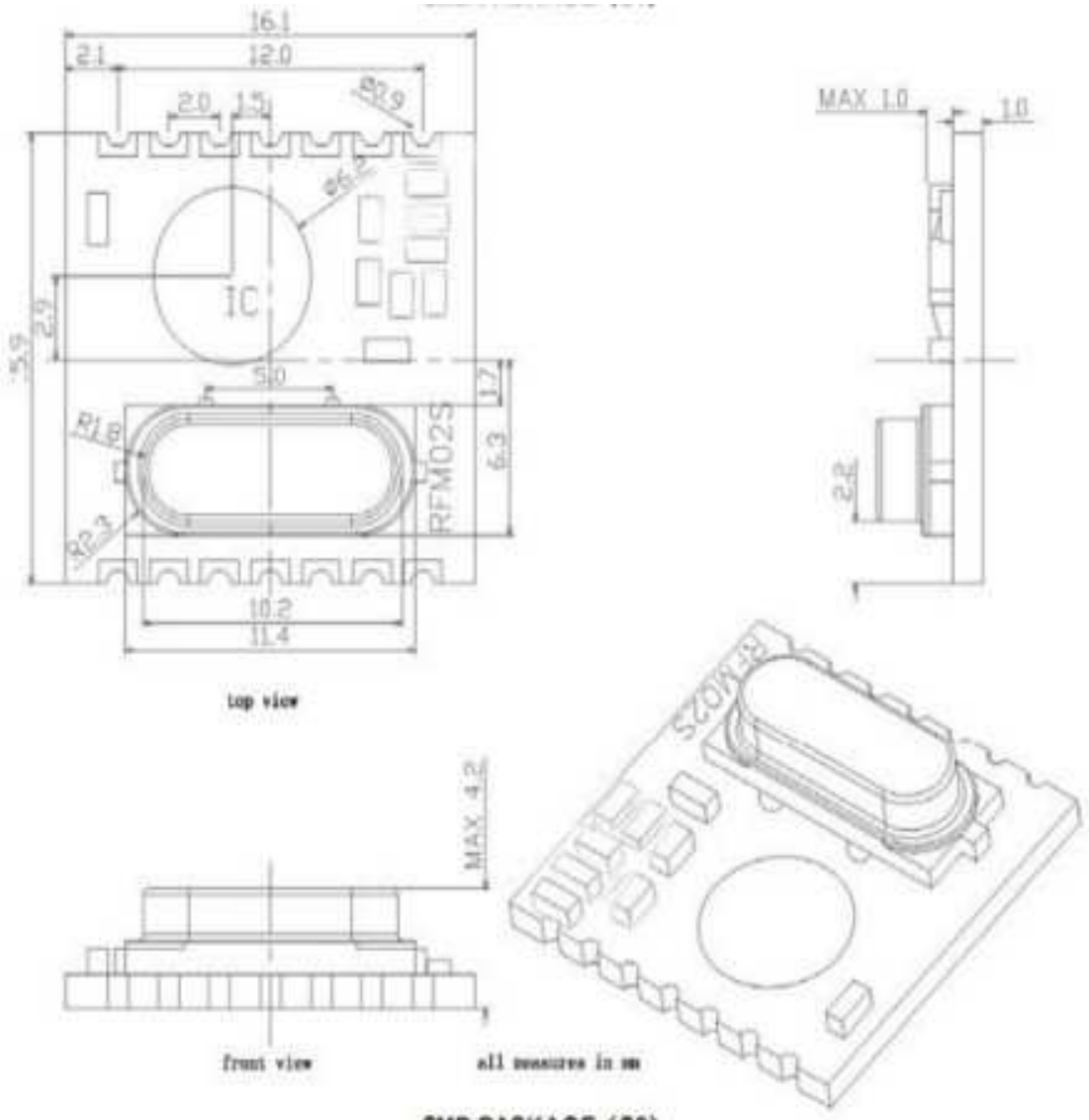
Site : 3m-chamber site
Condition : R&TTE 3m 3117 VERTICAL
EUT : #E

	Freq	Cable Loss	Antenna Factor	Preamp Factor	Read Level	Level	Limit Line	Over Limit
	MHz	dB	dB/m	dB	dBuV	dBuV/m	dBuV/m	dB
1 @	1820.000	1.66	30.70	44.60	69.20	56.87	77.00	-20.13
2	2719.000	2.09	32.81	44.83	64.43	54.49	77.00	-22.51

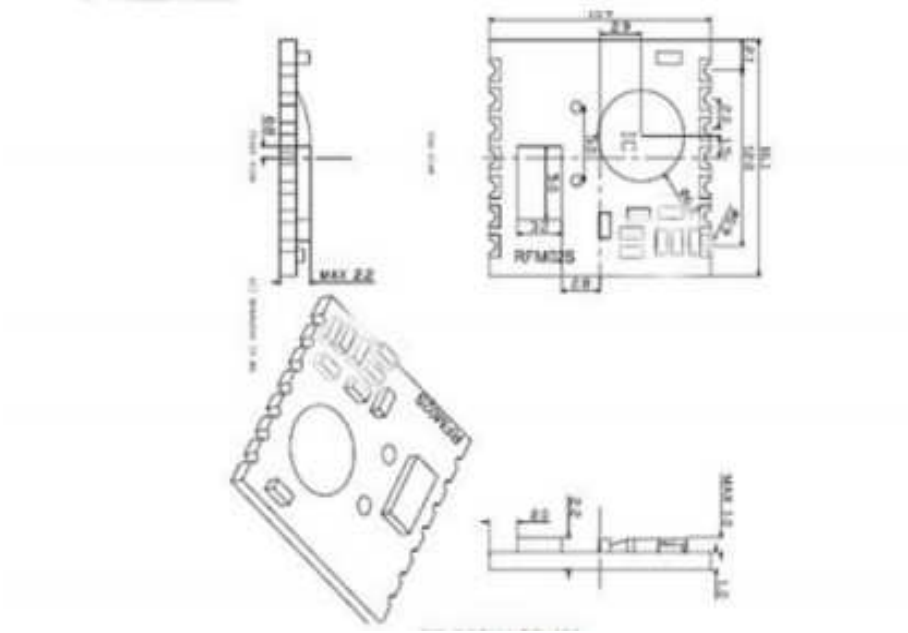
Mechanical Dimension:

（all dimensions in mm）

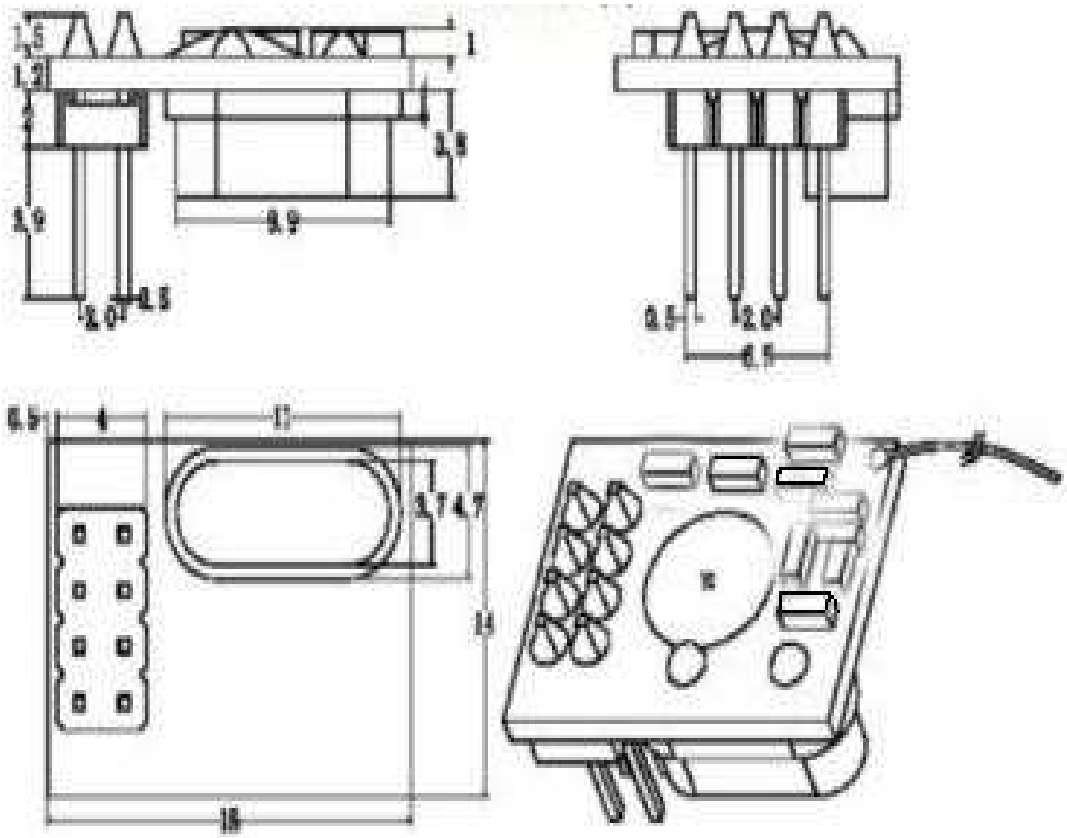
SMD PACKAGE（S1）



SMD PACKAGE（S2）



DIP PACKAGE（D）



Module Definition

model=module-operation_band-package_type

RFM02B-433-D

module type　operation band　Package

eg：1，RFM02 module at 433MHz band, DIP : RFM02-433-D。
2，RFM02 module at 868MHz band, SMD, thickness at 4.2mm : RFM02-868-S1。

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Sub-1GHz OOK / FSK High Performance RF Transmitter Module

Product Overview

RFM119B is a RF module with which +20dBm high power and high performance thus to support 127 to 1020 MHz frequency, OOK, (G) FSK modulation. The module is high integration so it simplifies the peripheral materials needed in the system design, so users can secondary development easily. The transmission power is up to +20 dBm, which can improves the link performance of the application, even can support a variety of packet formats and codec so as to flexibly meet the requirements of various applications for different data packet formats and coding.

RFM119B

Also, the RFM119B module can support 64-byte Tx FIFO, the GPIO and interrupt configuration, auto Tx running mode, low voltage detection, low frequency timing interrupt wake-up MCU, manual fast frequency hopping and so on, which making the application designs.more flexible thus to achieve product differentiation design. The working voltage of RFM119B is from 1.8 V to 3.6 V. The output power of +13dBm only consumes 23 mA emission current. It only consumes 80mA transmit current in the case of +20dBm output power. It is the best choice for low power and high efficiency.

Ordering Information

Module No.	Working Frequency
RFM119B-315S2	315MHz
RFM119B-433S2	433.92MHz
RFM119B-868S2	868.35MHz
RFM119B-915S2	915MHz

Features

- Comply with FCC and ETSI safety rules
- Strong anti-interference ability, suitable for complex interference environment scenarios
- Frequency range: 127~1020MHz
- Modulation and demodulation mode: OOK, (G) FSK &(G)MSK
- Data rate: 0.5~300 kbps
- Voltage Range: 1.8~3.6 V
- Transmit current
  - 23 mA @ 13 dBm，433.92 MHz, FSK
  - 80 mA @ 20 dBm，433.92 MHz, FSK
- Suppor tAuto Tx Mode
- Deep sleeping：300 nA
- Low power wake-up：800 nA
- 3-wire SPI interface
- Support direct and package mode
- Configurable packet processor& 64-Byte FIFO
- Support forward error correction

Applications

- Home security and building automation
- ISM band data communication
- Industrial monitoring and control
- Remote control and security system
- Remote key entry
- Wireless sensor nodes
- Labeling reader

Pin Information

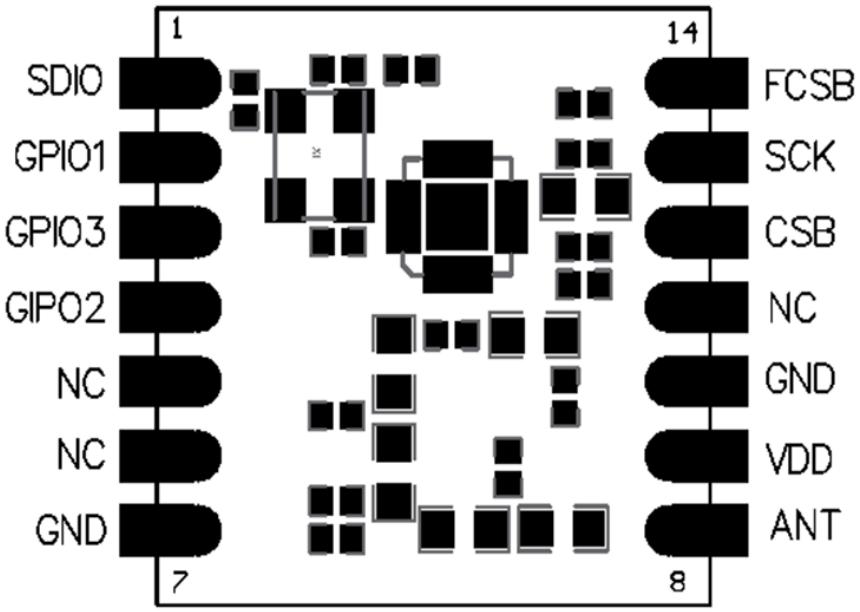


Figure 1. RFM119B Pin Assignment (Top View)

Table 1. RFM119B pin functions

Pin No.	Name	Description
1	SDIO	SPI Data input & output
2	GPIO1	Configurable as：DIN,INT1,INT2,DCLK(TX)
3	GPIO3	Configurable as：CLKO,DIN,INT2,DCLK(TX)
4	GPIO2	Configurable as：DIN,INT1,INT2,DCLK(TX)
5	NC	Not connected
6	NC	Not connected
7	GND	Ground
8	ANT	antenna
9	VDD	Positive power supply
10	GND	Ground
11	NC	Not connected
12	CSB	SPI Selection to access registers
13	SCK	SPI clock
14	FCSB	SPI selection to access FIFO

Electrical parameters

Testing conditions: Power supply 3.0V, temperature 25 ℃

Recommended operating conditions

Table 2. Recommended Operating Conditions

Parameter	Symbol	Conditions	Minimum	Maximum	Unit
Supply Voltage	V_{DD}		1.8	3.6	V
Operating Temperature	T_{OP}		-40	85	℃
Power Supply Voltage Slope			1		mV/us

Absolute Maximum Rating

Table 3. Absolute Maximum Rating

Parameter	Symbol	Conditions	Minimum	Maximum	Unit
supply voltage	V_{DD}		-0.3	3.6	V
Interface voltage	V_{IN}		-0.3	3.6	V
junction temperature	T_J		-40	125	℃
Storage temperature	T_{STG}		-50	150	℃
Soldering temperature	T_{SDR}	Lasting 30s at least		255	℃
ESD Level[2]		HBM	-2	2	kV
Latch current		@ 85 ℃	-100	100	mA

DC Characteristics

Table 4. DC characteristics

Parameter	Conditions	Minimum	Typical	Maximum	Unit
RFM119B Working Conditions	315MHz band, Pout =+20dBm		80	85	mA
	433MHz band, Pout =+20dBm		85	90	mA
	868MHz band, Pout =+20dBm		85	90	mA
	915MHz band, Pout =+20dBm		80	85	mA
RFM119B sleep current	full band			2	uA
RFM119B Working band	Different matching networks are needed	760	868、915	1020	MHz
		380	433.92	510	MHz
		190	315	340	MHz

Parameter	Conditions	Minimum	Typical	Maximum	Unit
		127		170	MHz
FSK data rate		0.5		300	kbps
OOK data rate		0.5		40	kbps
FSK Frequency deviation range		2		200	KHz
Frequency deviation resolution			25		Hz

Typical Application

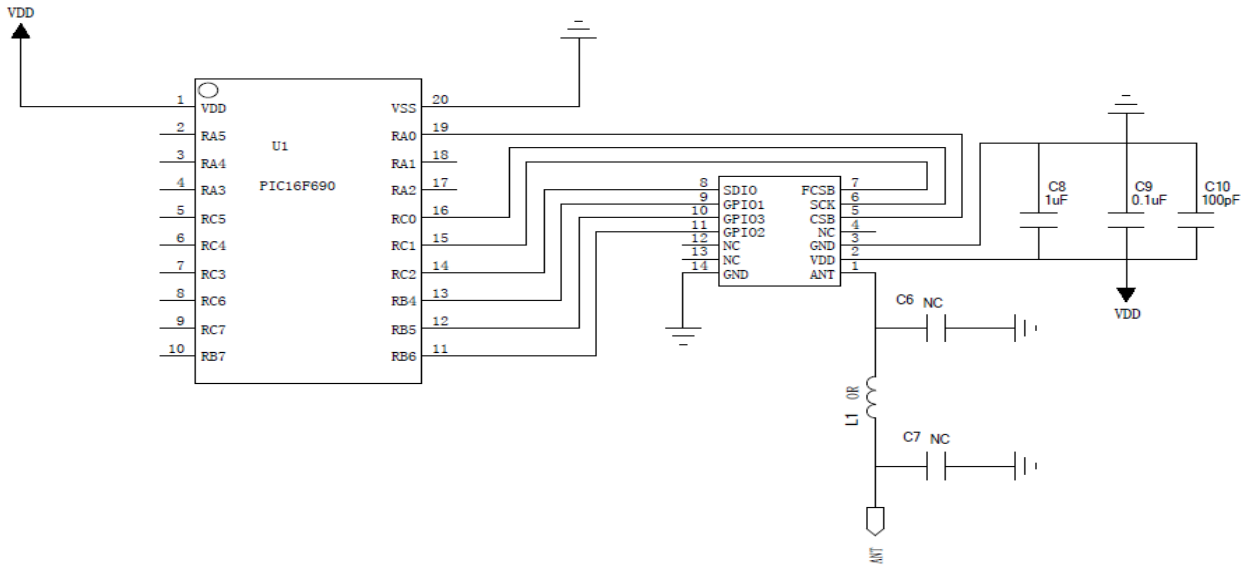
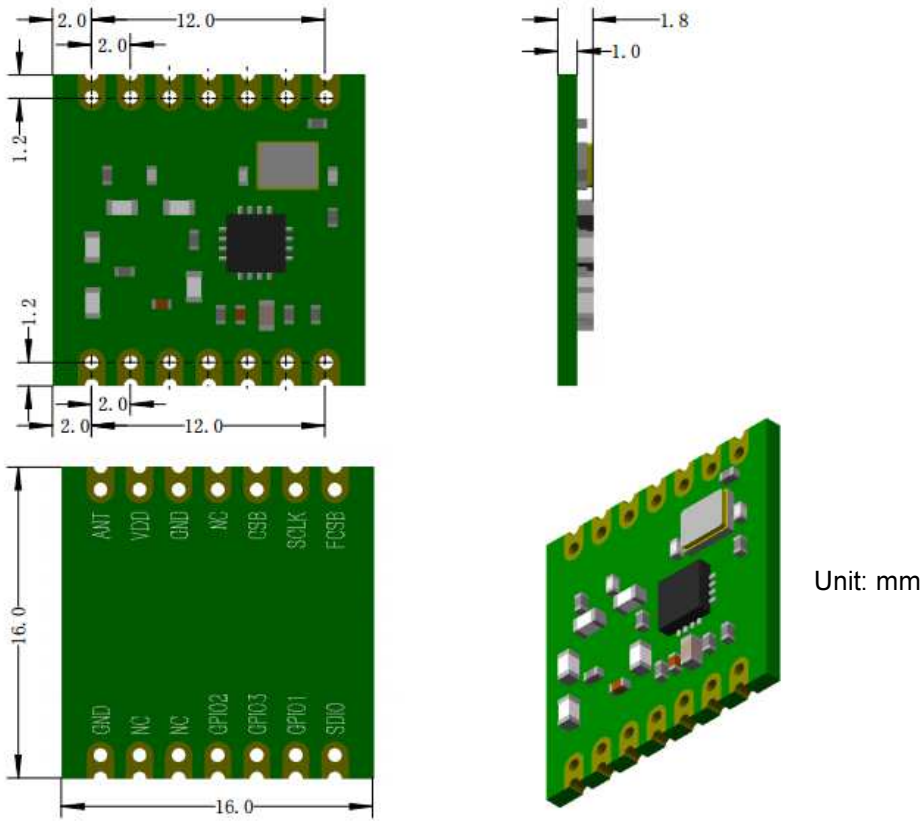


Figure 2. RFM119B Application Reference Diagram

For software information, please refer to the chip datasheet and demo program of HopeDuino™ development kit

Dimensions



Unit: mm

Figure3. Dimensions

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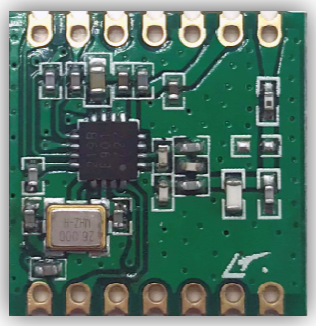
Sub-1GHz OOK / FSK High Performance RF Transmitter Module



RFM219B

Product Overview

RFM219B is a low power, high performance, OOK, (G) FSK RF receiver module which suitable for all kinds of 127 to 1020 MHz wireless applications. RFM219B is highly integrated, which simplifies the peripheral materials that needed in system design. It supports a variety of packet formats and codec methods, and can flexibly meet the needs of various applications for different packet formats and e codec. Also, the RFM219B module can support 64-byte Rx FIFO, the GPIO and interrupt configuration, Duty-Cycle running mode, RSSI detection, low voltage detection, low consumption timing out out wake-up, manual fast frequency hopping, static noise output and so on, which making the application designs more flexible thus to achieve product differentiation design.RFM219B works from 1.8 V to 3.6V. With -120dBm sensitivity and current consumption of only 8.5 mA, which combined with Duty-Cycle mode, so the receiving power of chips can be further reduced.

Ordering Information

Module No.	Working Frequency
RFM219B- 315S2	315MHz
RFM219B- 433S2	433.92MHz
RFM219B- 868S2	868.35MHz
RFM219B- 915S2	915MHz

Features

- Comply with FCC and ETSI safety rules
- Strong anti-interference ability, suitable for complex interference environment scenarios
- Frequency range: 127~1020MHz
- Modulation and demodulation mode: OOK, (G)FSK &(G)MSK
- Data rate: 0.5~300 kbps
- Sensitivity：
  - -120 dBm @ 2.0kbps, F_{RF} = 433.92
  - -111dBm @ 50kbps, F_{RF} = 433.92
- Voltage range： 1.8 ~ 3.6 V
- Receiving current： 8.5 mA @ 433.92 MHz
- Support ultra low power reception mode
- Deep sleep mode：300 nA，Duty Cycle OFF
- Low power time mode：800 nA，Duty Cycle ON
- 3-wire SPI interface
- Support for direct and package mode
- Configurable packet processor and 64-Byte FIFO
- Support non return to zero, Manchester, data whitening decoding
- Support forward error correction

Applications

- Automatic meter reading
- Home security and building automation
- ISM band data communication
- Industrial monitoring and control
- Remote control and security system
- Remote key entry
- Wireless sensor nodes
- Labeling reader

Pin Information

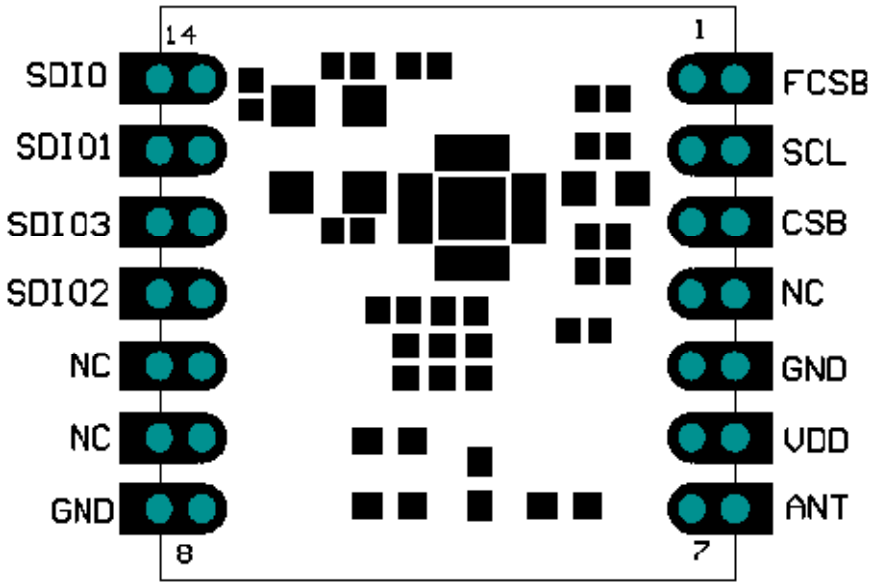


Figure1. RFM219B Pin Assignment (Top View)

Table1. RFM219B Pin Functions

Pin No.	Name	Description
1	FCSB	SPI Selection to access FIFO
2	SCL	SPI clock
3	CSB	SPI Selection to access registers
4	NC	Not connected
5	GND	Ground (electricity)
6	VDD	Positive power supply
7	ANT	Antenna Input
8	GND	Ground (electricity)
9	NC	Not connected
10	NC	Not connected
11	SDIO2	Configurable as：INT1，INT2，DOUT，DCLK，RF_SWT
12	SDIO3	Configurable as：CLKO， DOUT， INT2， DCLK
13	SDIO1	Configurable as：DOUT，INT1，INT2，DCLK，RF_SWT
14	SDIO	SPI Data input & output

Electrical Parameters

Testing conditions: Power supply 3.0V, Temperature 25 ℃

Table2. Recommended Operating Conditions

Parameter	Symbol	Conditions	Minimum	Typical value	Maximum	Unit
Supply Voltage	VDD		1.8	3.3	3.6	V
Operating Temperature	T		-40		85	℃
Power Supply Voltage Slope			1			mV/us

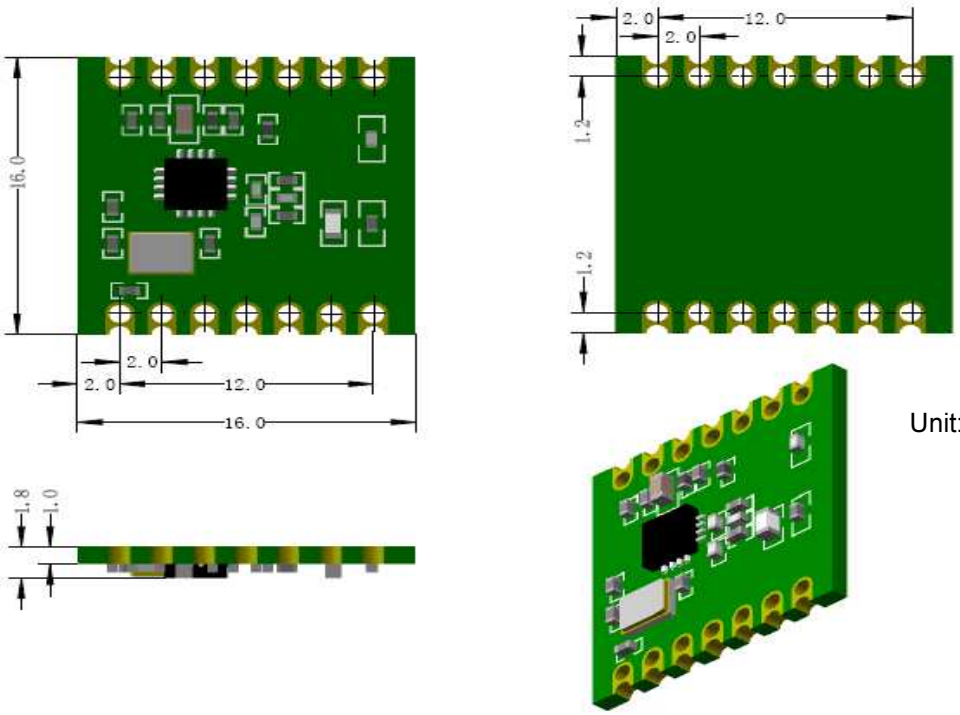
Table3. Absolute Maximum Rating

Parameter	Symbol	Conditions	Minimum	Maximum	Unit
Supply Voltage	VDD	-0.3	-0.3	3.6	V
Interface Voltage	VIN	-0.3	-0.3	3.3	V
Junction Temperature	TJ	-40	-40	125	℃
Storage Temperature	TSTG	-50	-50	150	℃
Soldering Temperature	TSDR	Last for at least 30s		255	℃
ESD Level[2]	HBM	-2	-2	2	kV
Latch Current	@ 85 ℃	-100	-100	100	mA

Table4. Receiving Parameters

Parameter	Conditions	Minimum	Typical value	Maximum	Unit
Frequency Band	Different matching networks are needed	760	868、915	1020	MHz
		380	433.92	510	MHz
		190	315	340	MHz
		127		170	MHz
Receiving Sensitivity FSK F_{DEV} =10 kHz, DR =2.0 kbps	433MHz 868MHz 915MHz	- - -	-121 -119 -117	- - -	dBm

Dimensions



Unit: mm

Figure 2.Dimensions

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